

QHRAE

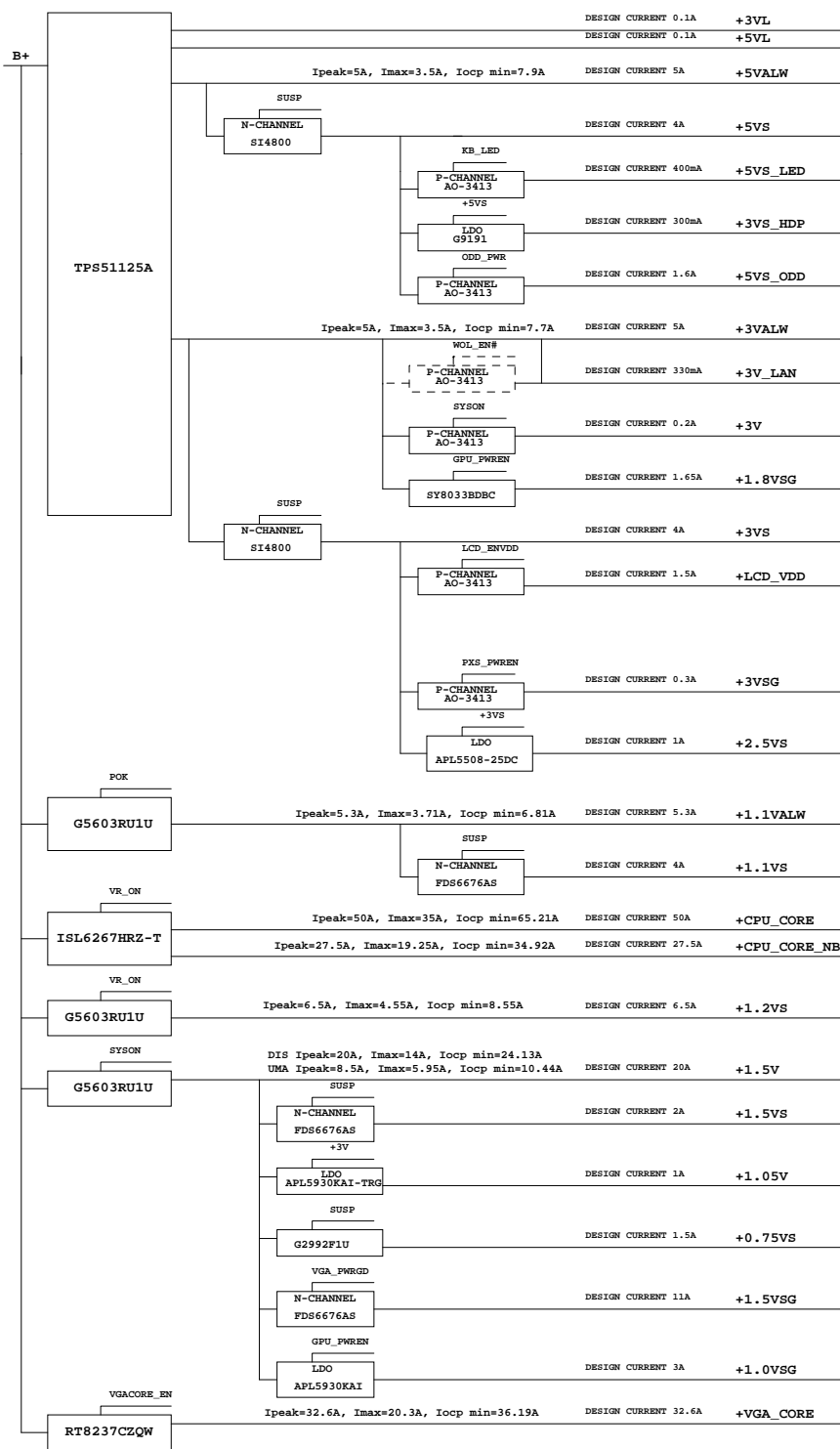
Superior 10AS/10ASG

LA-7213P REV 1.0 Schematic

AMD Llano FS1 Processor / Hudson M2/M3
Whistler Pro

2011-04-30 Rev 1.0

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Voltage Rails

(O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB +VGA_CORE +3VSG +1.8VSG +1.5VSG +1.0VSG
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	HDMI				SKU		
description	HDMI				SKU		
explain	UMA PowerXpress	Discrete	COMMON	CEC	UMA	PowerXpress	Discrete
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	UMA@	UMA@+VGA@+PXS@	VGA@+DIS@

Function		LAN		CIR	KB Light
description		LAN		CIR	KB Light
explain		10/100M	GIGA	CIR	KB Light
BTO		8105E@	8111E@	CIR@	KBL@

Function		G-SENSOR	Cam & Mic	Panel		
description		G-SENSOR	Cam & Mic	Panel (DIS@)		
explain		G-SENSOR	Cam & Mic	3D LVDS	eDP	Non-3D & EDP
BTO		GSENSOR@	CAM@	3D@+NOEDP@	EDP@	NO3D@+NOEDP@

Function	GPIO for PowerXpress		Chipset			
description	PowerXpress (PXS@)		FCH		GPU	
explain	PowerXpress Enable	Crossfire Enable	Hudson-M3		Whistler Pro	
BTO	PXSEN@	CROSSEN@	HUDM3R1@	HUDM3R3@	WHPROR1@	WHPROR3@

Function	PowerXpress		Renesas USB3.0	FCH		EC	
description	PowerXpress (PXS@)		Renesas USB3.0	FCH		EC	
explain	BACO mode	Non-BACO	Renesas USB3.0	Hudson-M2	Hudson-M3	KB-930	KB-9012
BTO	BACO@	NOBACO@	RENE@	M2@	M3@	KB930@	KB9012@

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN		
+3VS	3G		

EC SM Bus1 Address



EC SM Bus2 Address

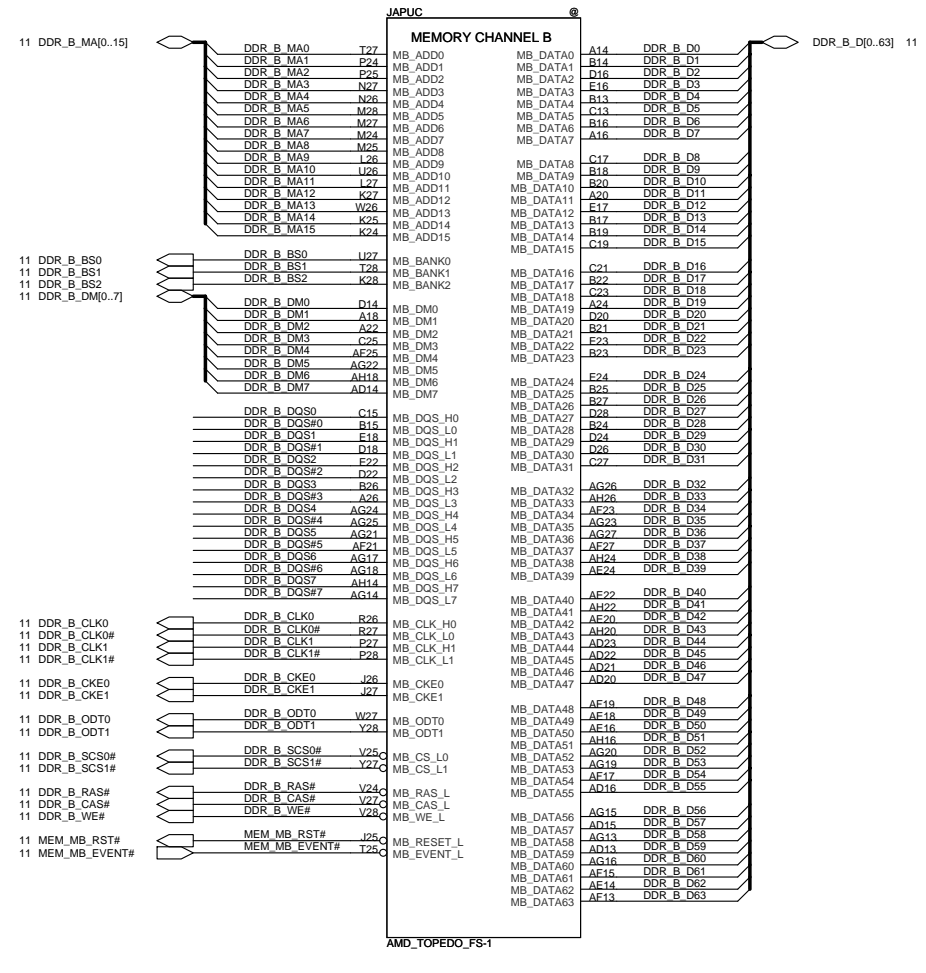
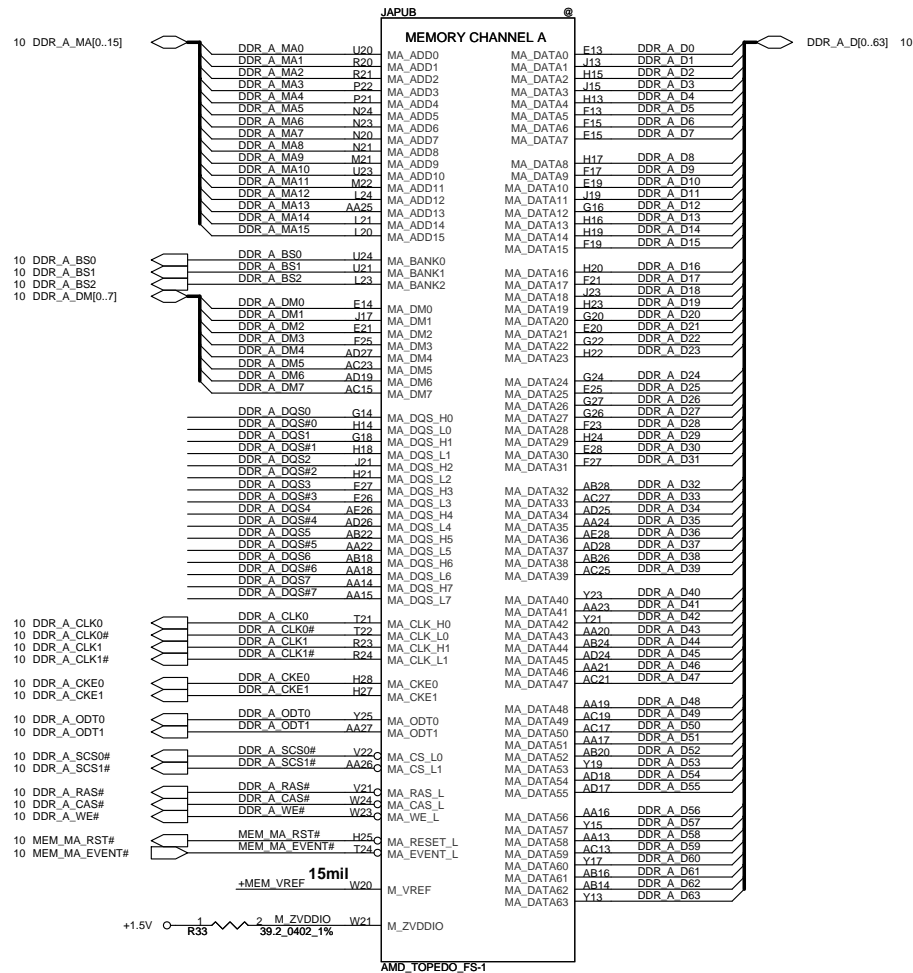
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	CPU Thermal Sensor	98 H	1001 1001 b
+3VL	HDMI-CEC	34 H	0011 0100 b	+3VS	GPU Thermal Sensor	41 H	0100 0001 b
				+3VS	G-Sensor	40 H	0100 0000 b
				+3VS	Light Sensor	52 H	0101 0010 b
Power	Device	HEX	Address	+3VS	3D - Bootloader	C0 H	1100 0000 b
+3VL	Cap. Sensor		Virtual I2C	+3VS	3D - Slave	C0 H	1100 0000 b

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

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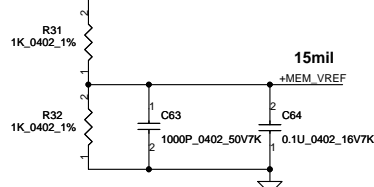
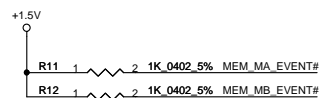
10 DDR_A_DQS[0..7] 
10 DDR_A_DQS#[0..7] 

11 DDR_B_DQS[0..7] 
11 DDR_B_DQS#[0..7] 

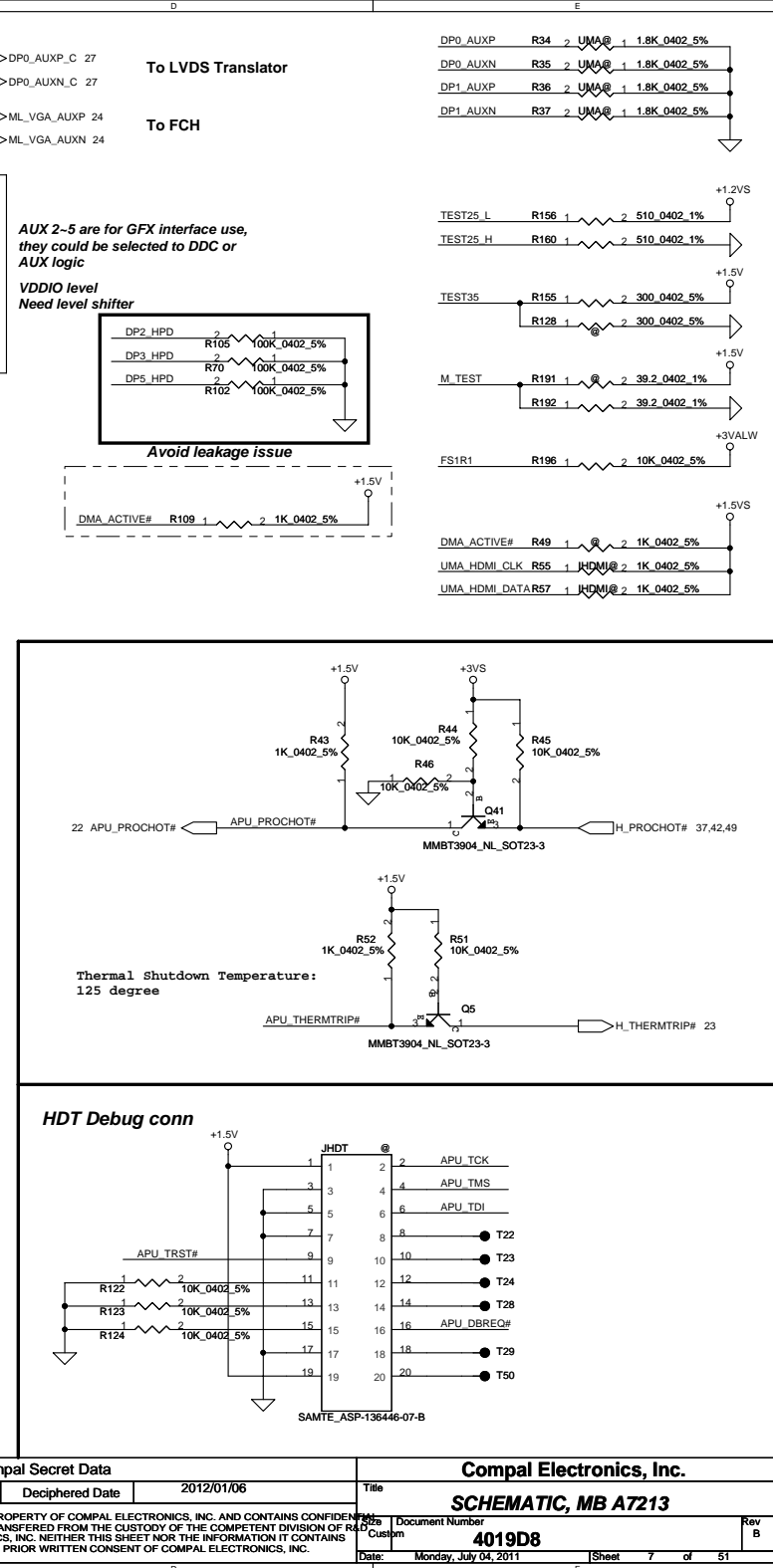
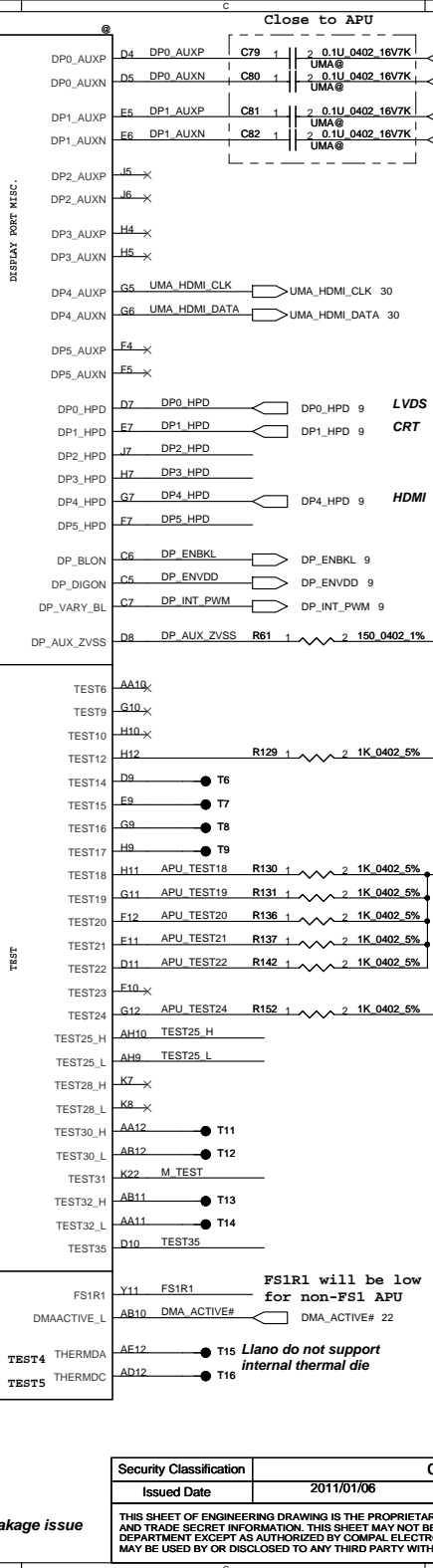


EVENT# pull high

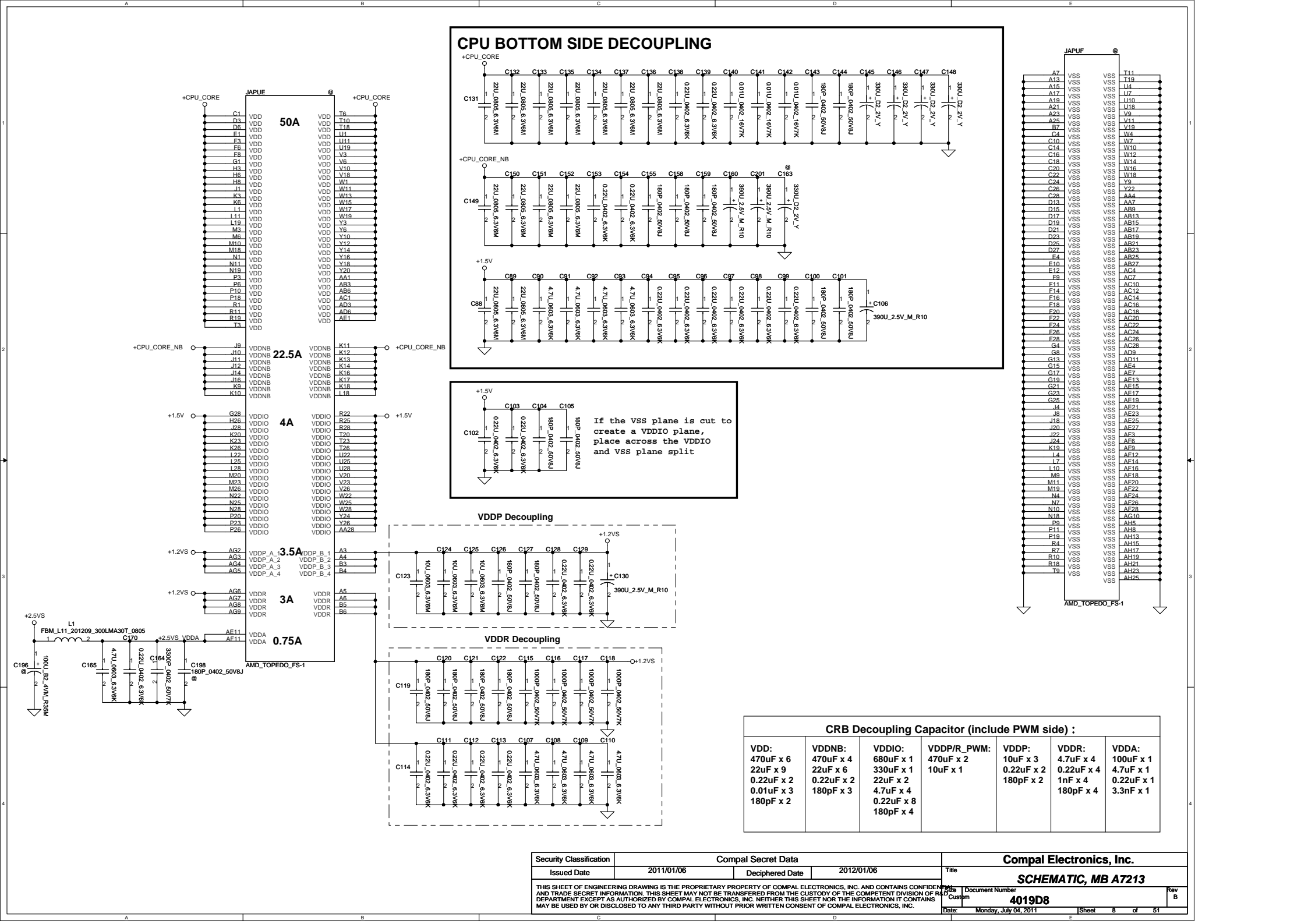
0.75V Reference Voltage



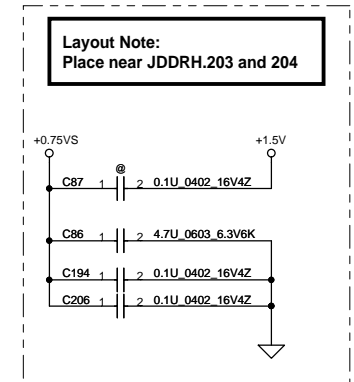
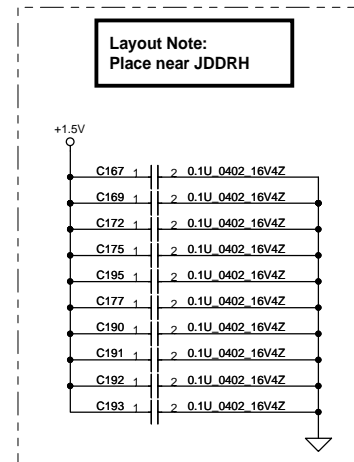
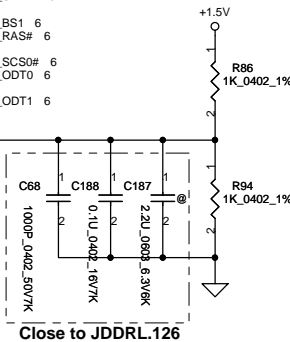
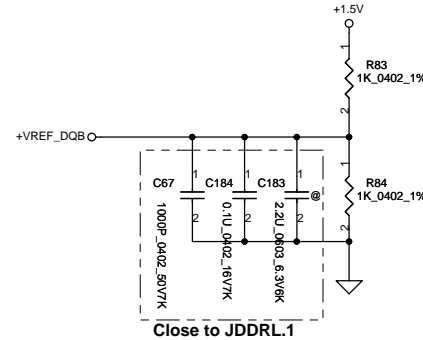
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DDR3 SO-DIMM B Standard Type

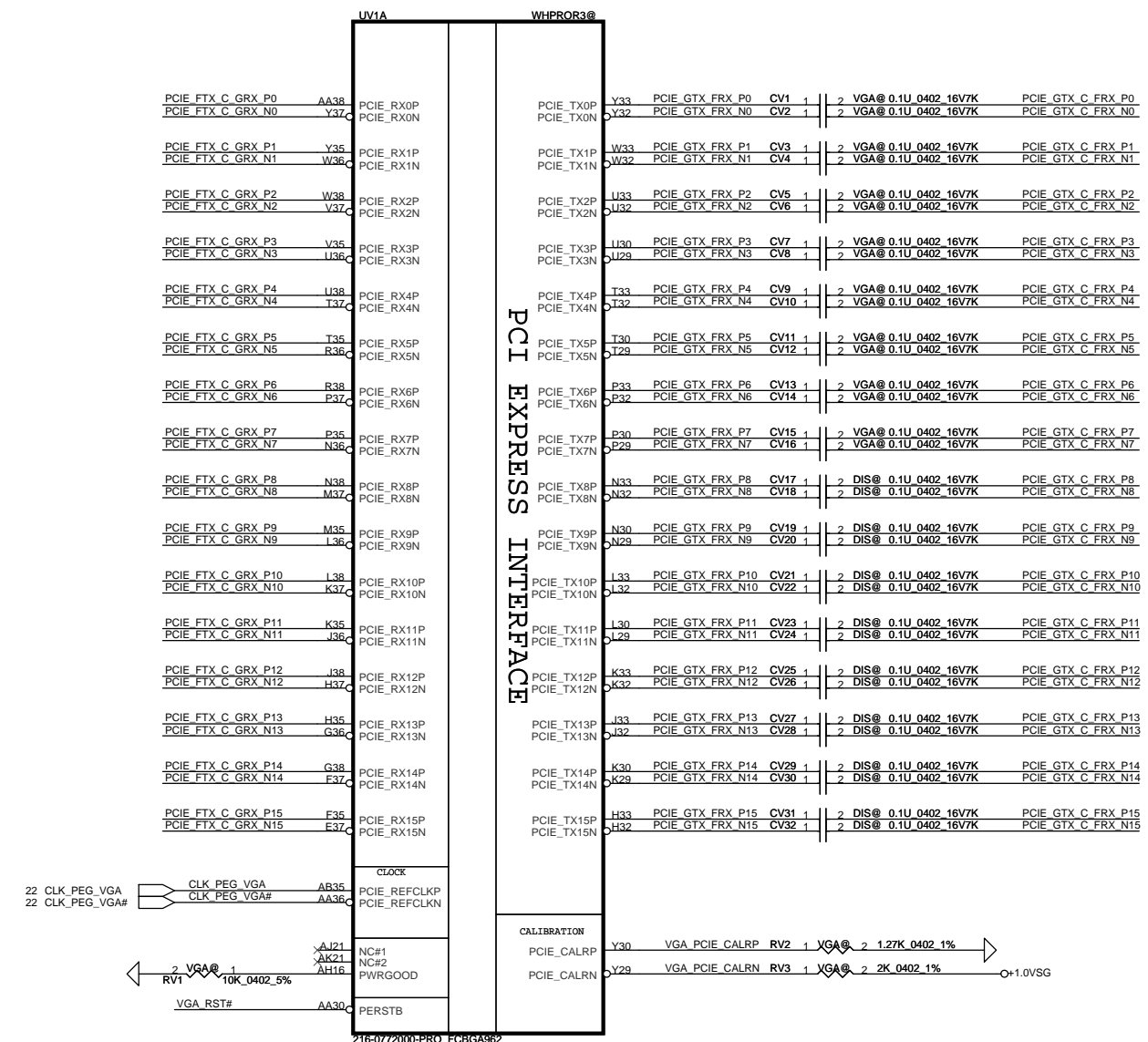


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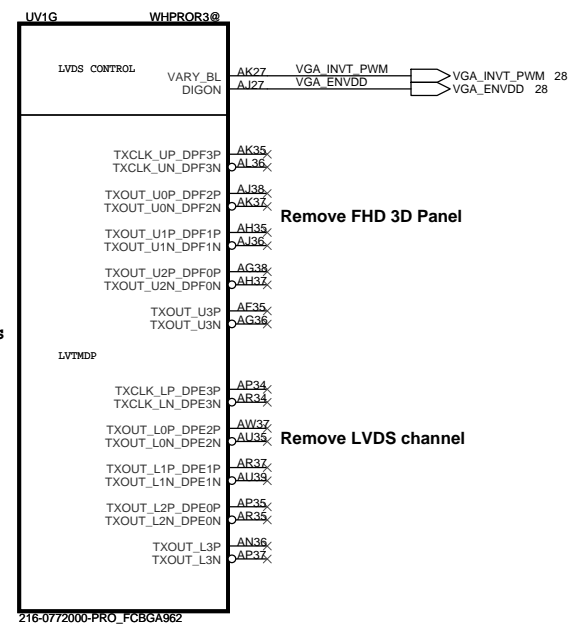
5 PCIE_FTX_C_GRX_P[0..15] PCIE_FTX_C_GRX_P[0..15]
5 PCIE_FTX_C_GRX_N[0..15] PCIE_FTX_C_GRX_N[0..15]

PCIE GTX_C_FRX_P[0..15] PCIE GTX_C_FRX_P[0..15] 5
PCIE GTX_C_FRX_N[0..15] PCIE GTX_C_FRX_N[0..15] 5

VGA_INVT_PWM 1 RV4 10K_0402_5%
VGA_ENVDD 1 RV5 10K_0402_5%

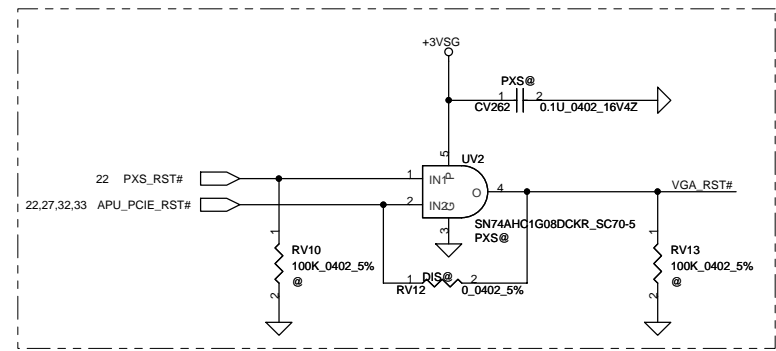


For PowerXpress

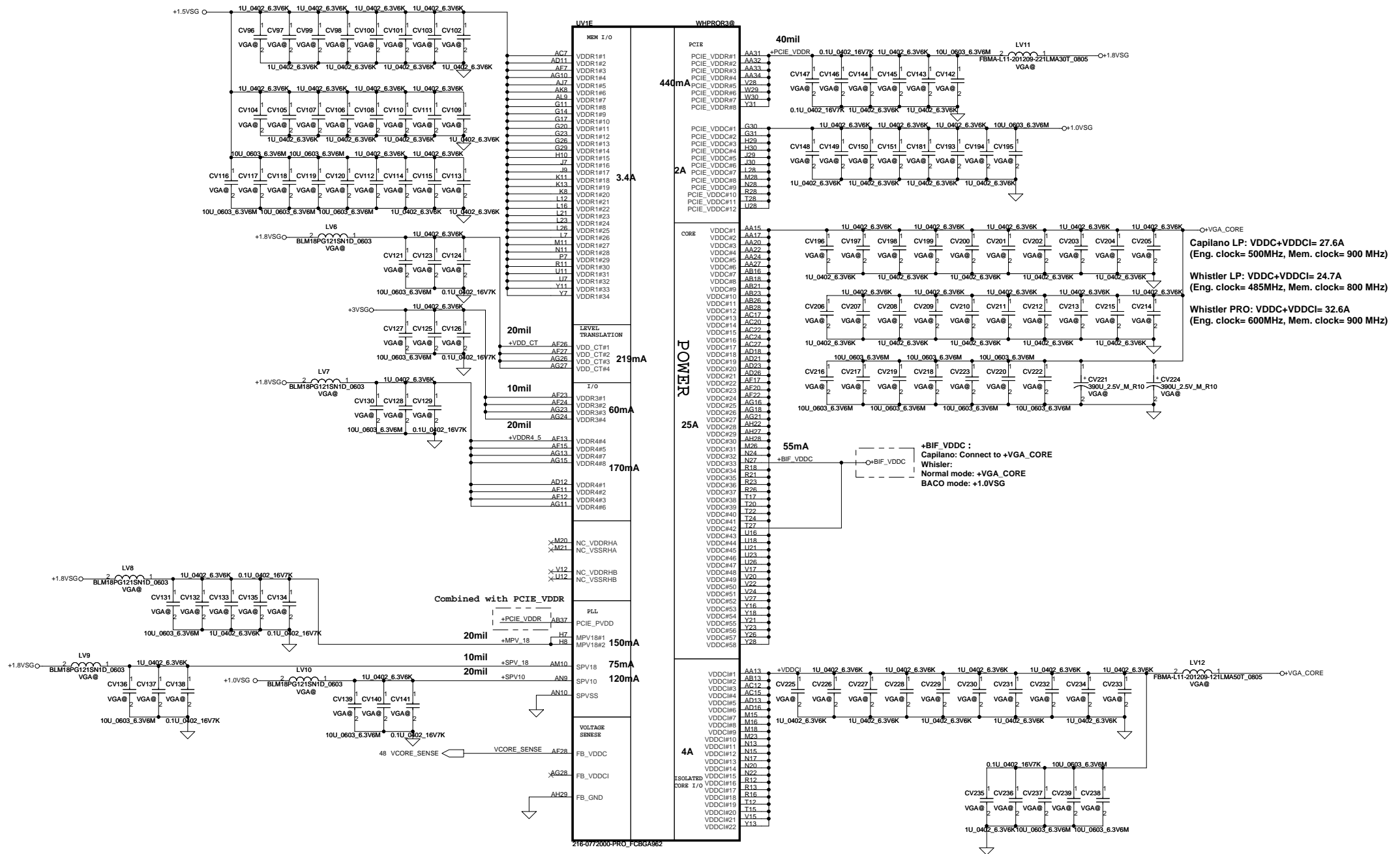


Remove FHD 3D Panel

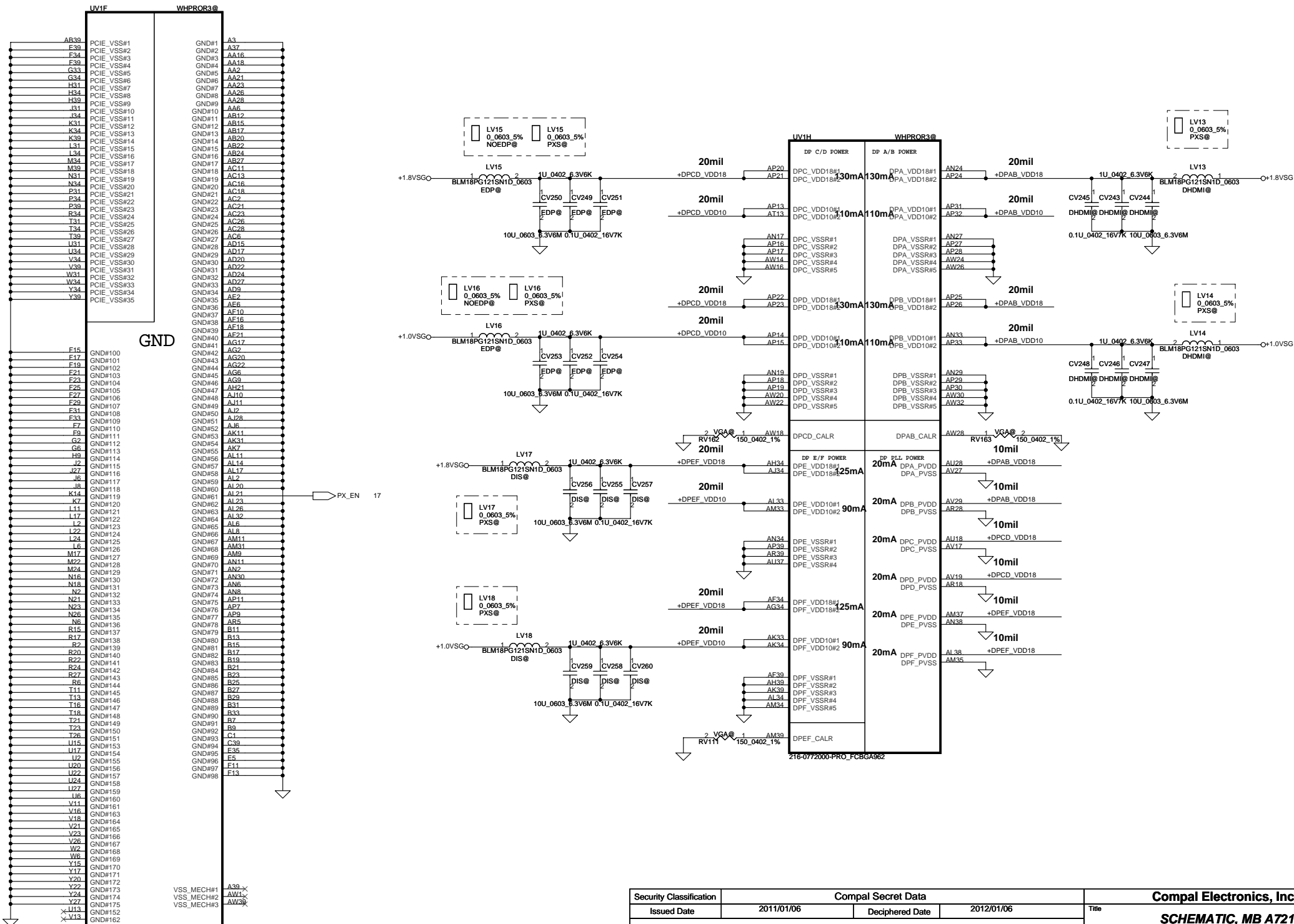
Remove LVDS channel

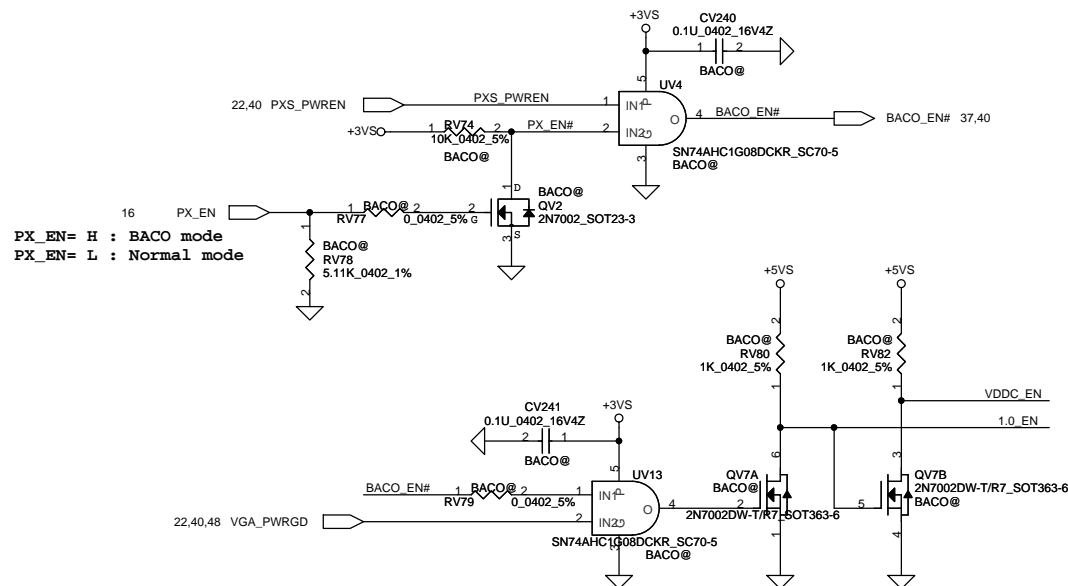


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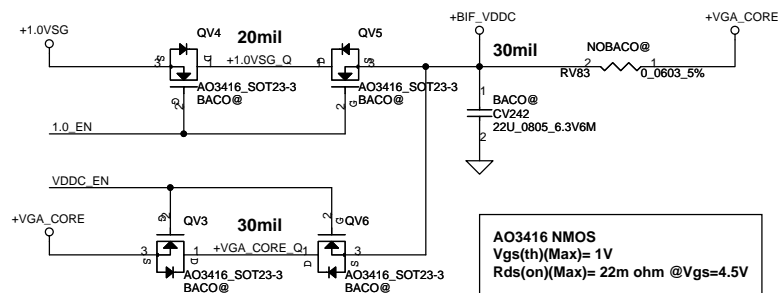
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BACO mode:
+VGA_CORE: off
+1.5VSG: off
+BIF_VDDC= +1.0VSG

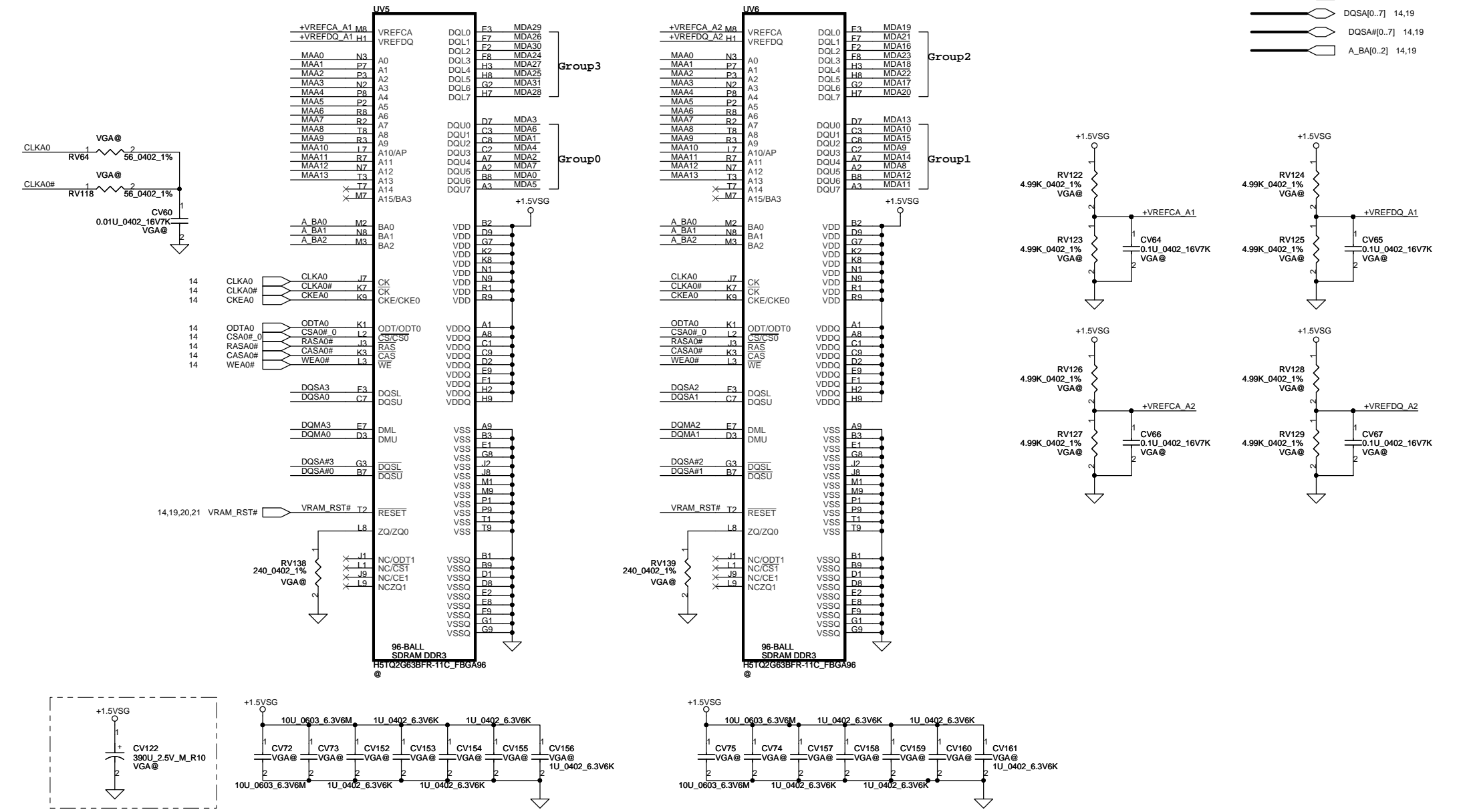
Normal mode:
+BIF_VDDC= +VGA_CORE



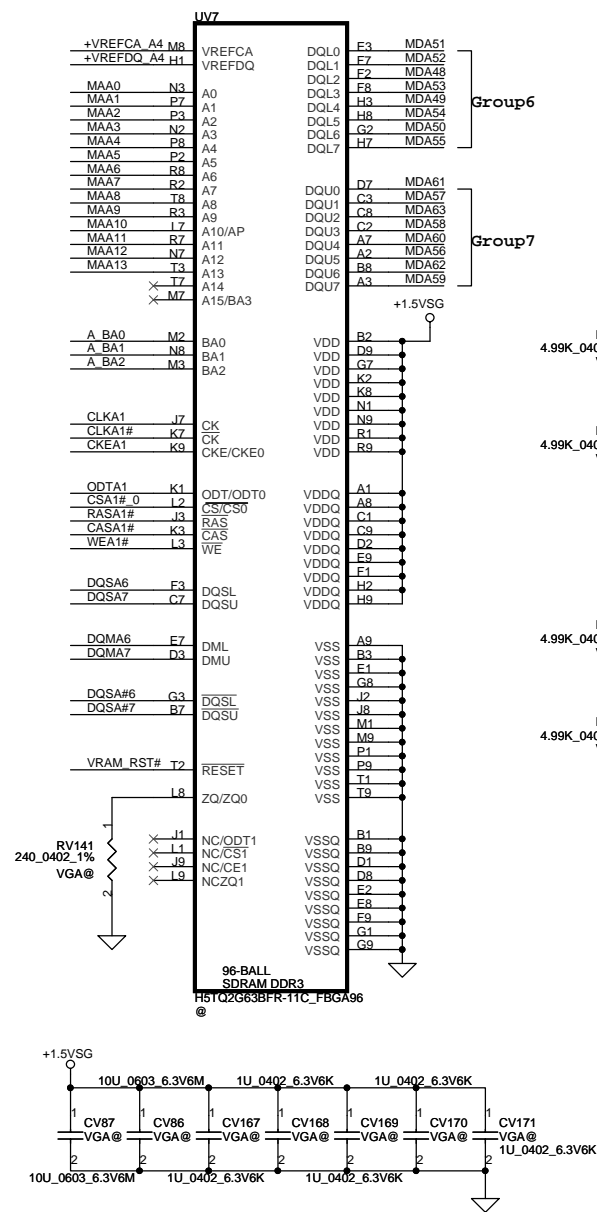
AO3416 NMOS
Vgs(th)(Max)= 1V
Rds(on)(Max)= 22m ohm @Vgs=4.5V

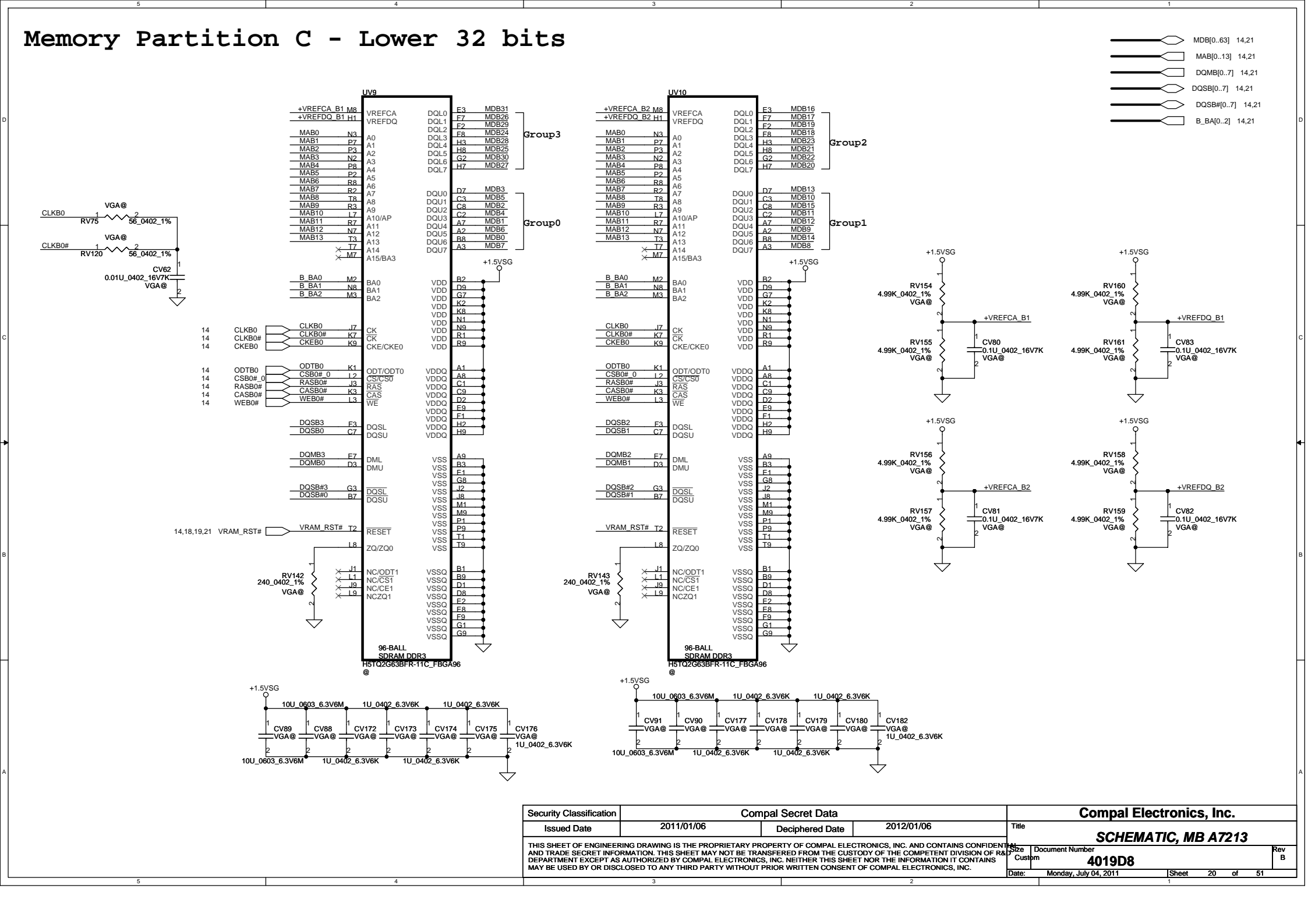
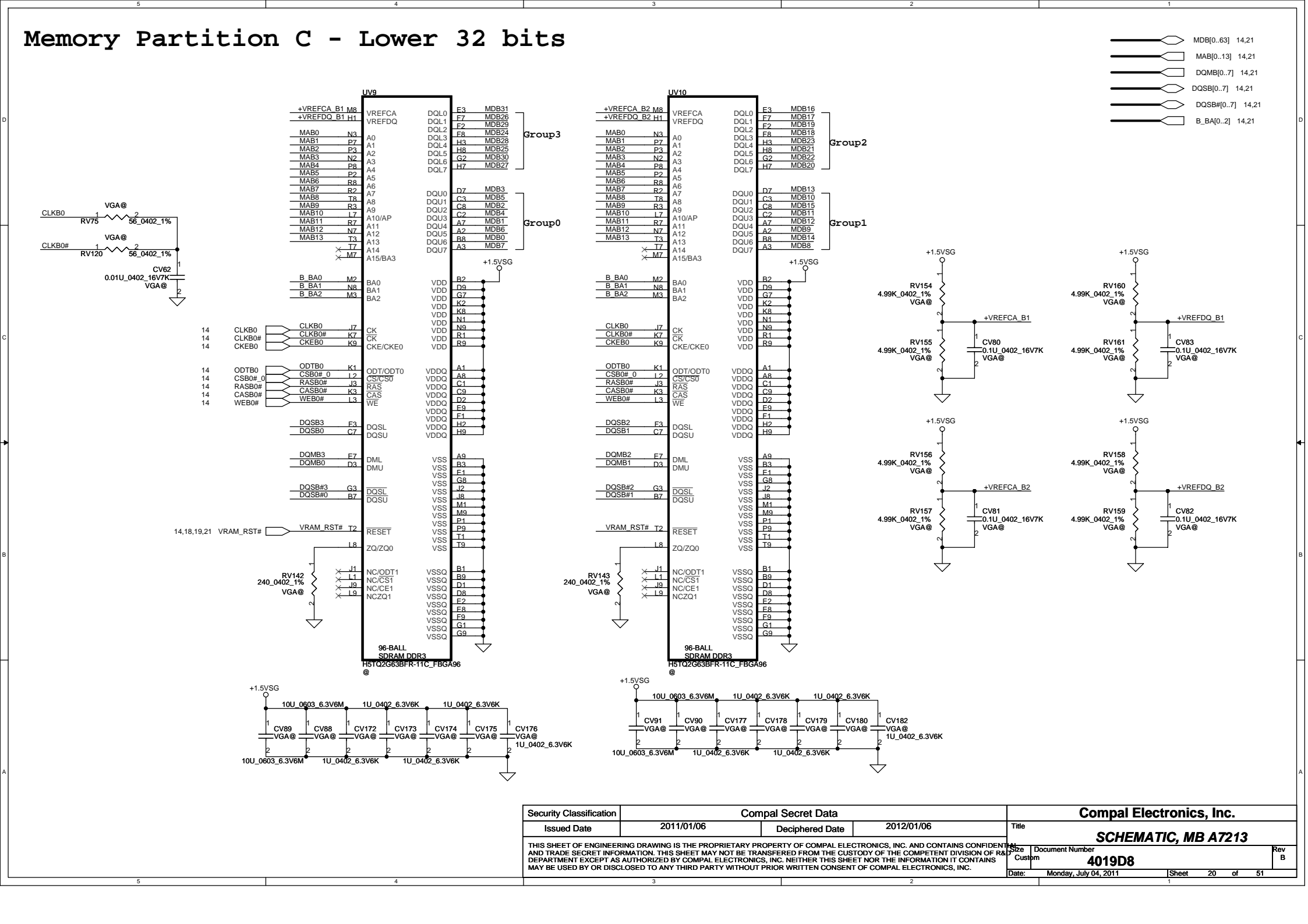
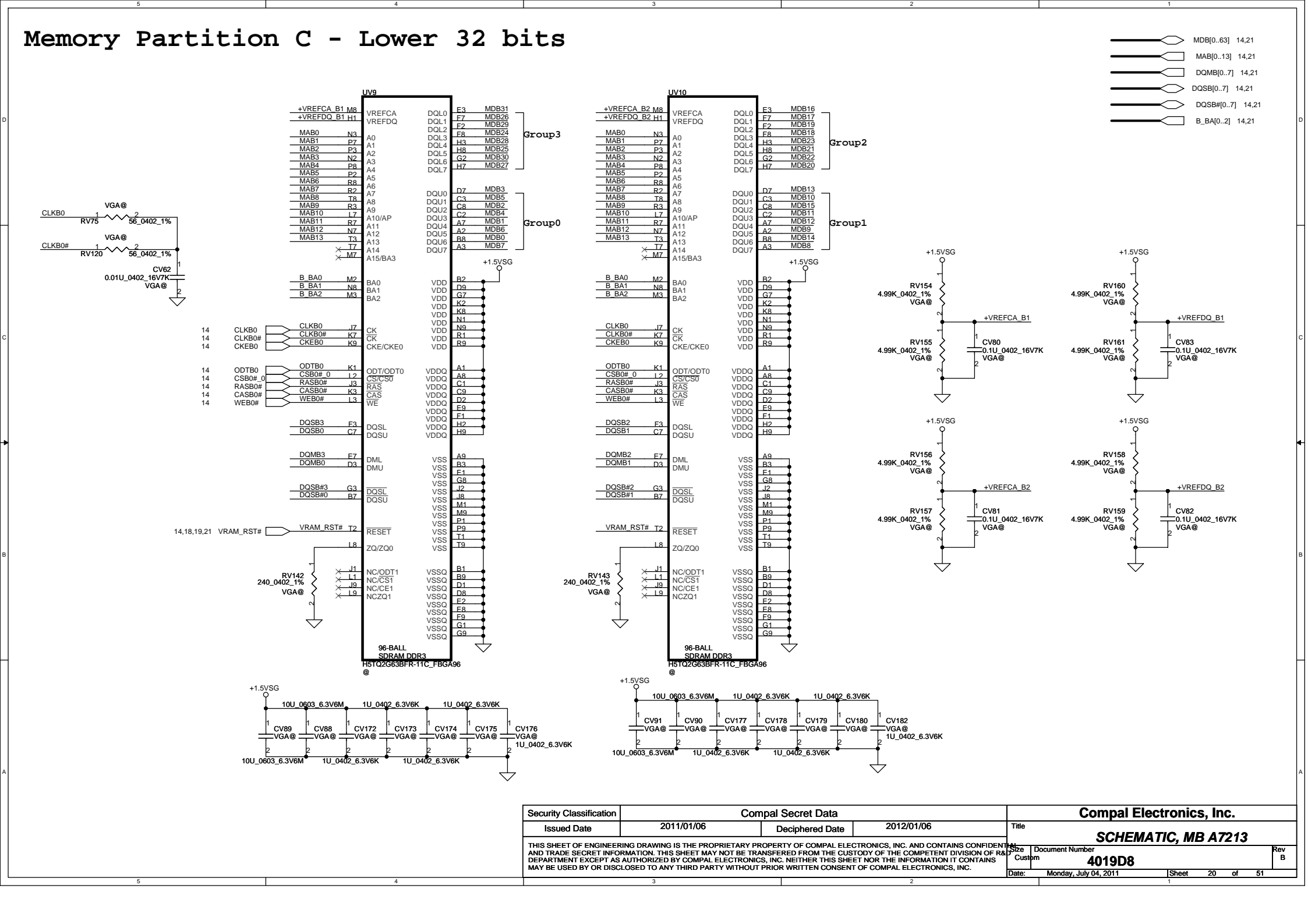
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Memory Partition A - Lower 32 bits

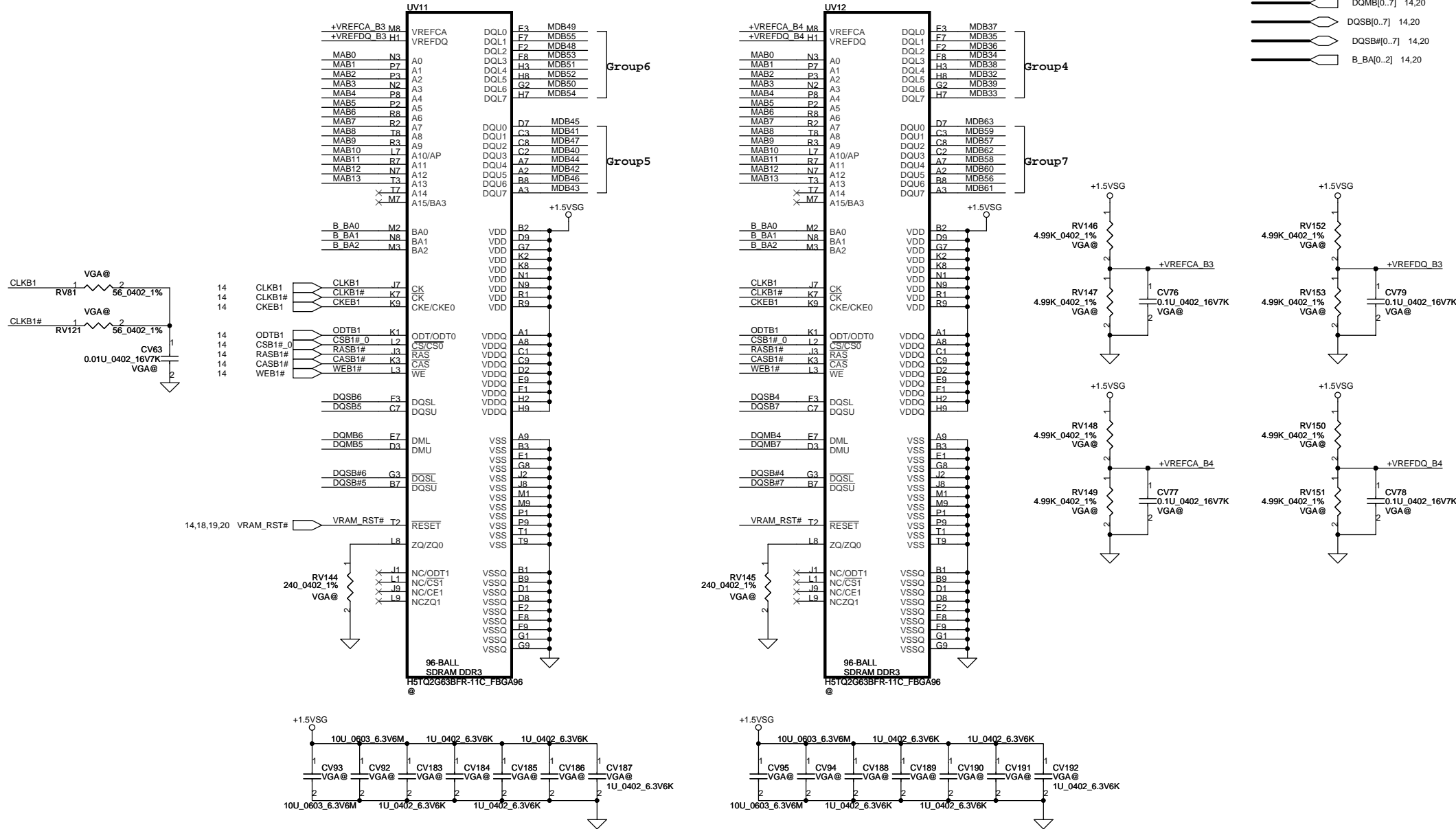


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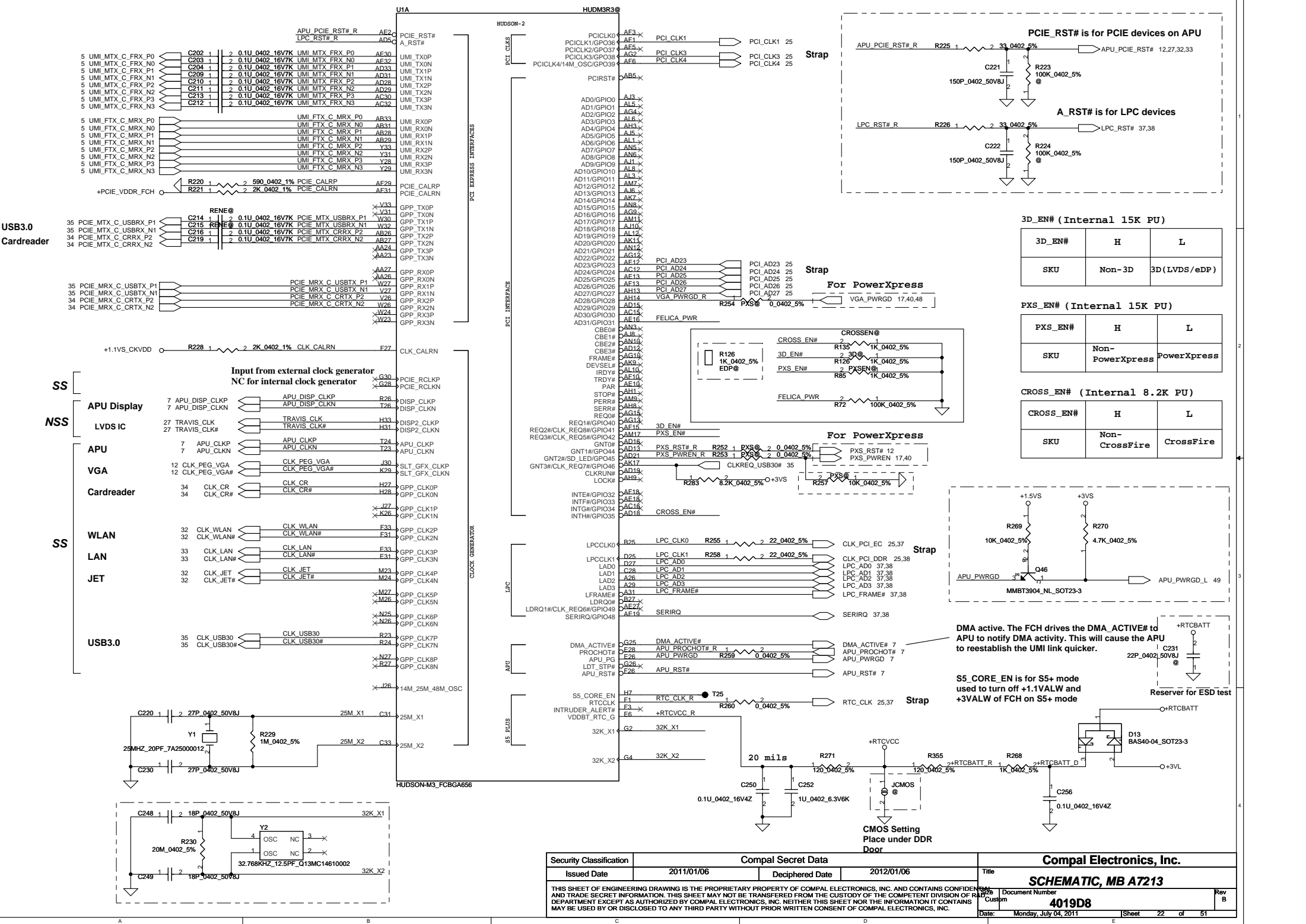
[illegible][illegible]

[illegible][illegible]

Memory Partition C - Upper 32 bits



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3D_EN# (Internal 15K PU)

3D_EN#	H	L
SKU	Non-3D	3D (LVDS/eDP)

PXS_EN# (Internal 15K PU)

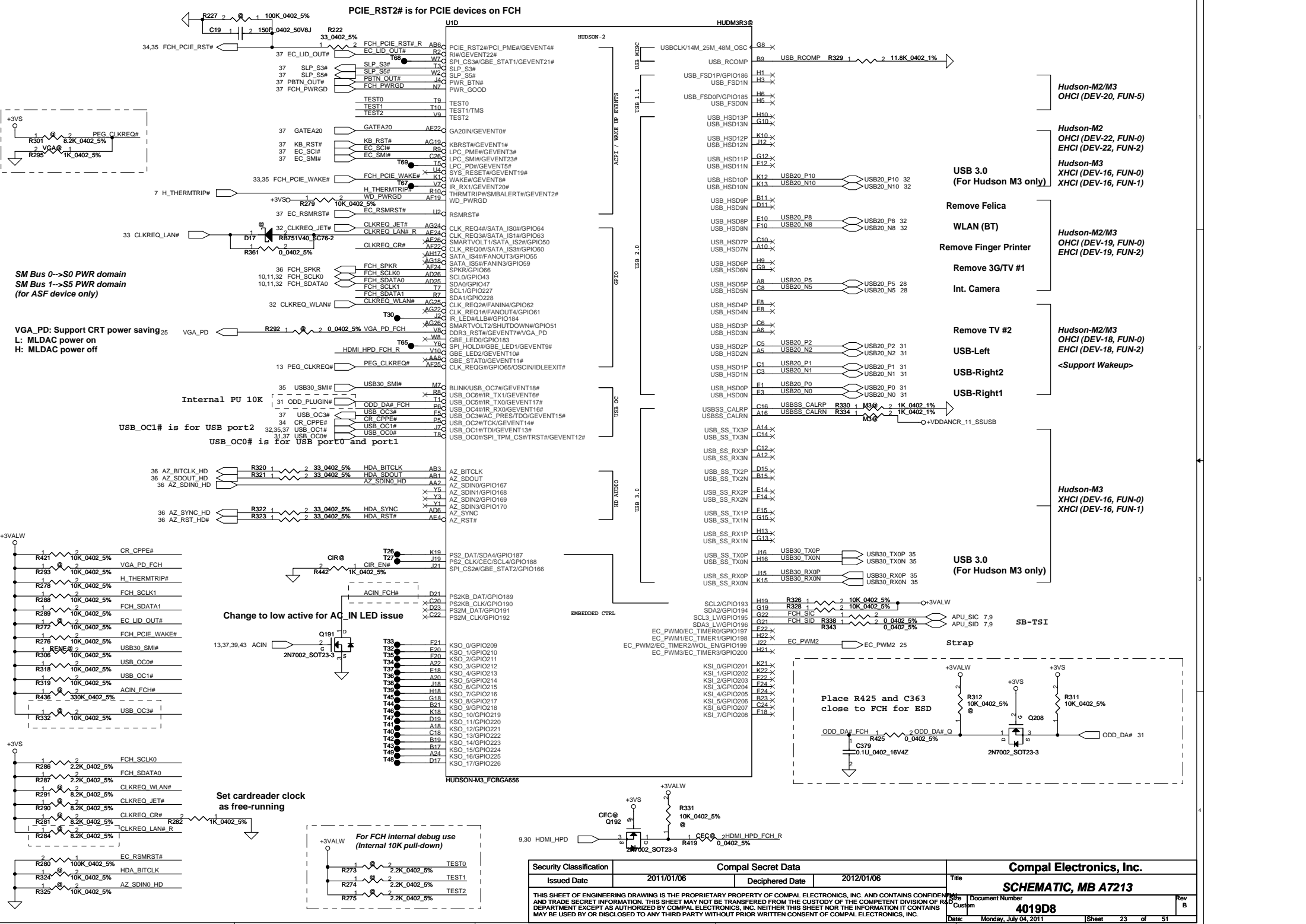
PXS_EN#	H	L
SKU	Non-PowerXpress	PowerXpress

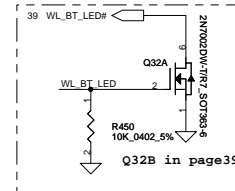
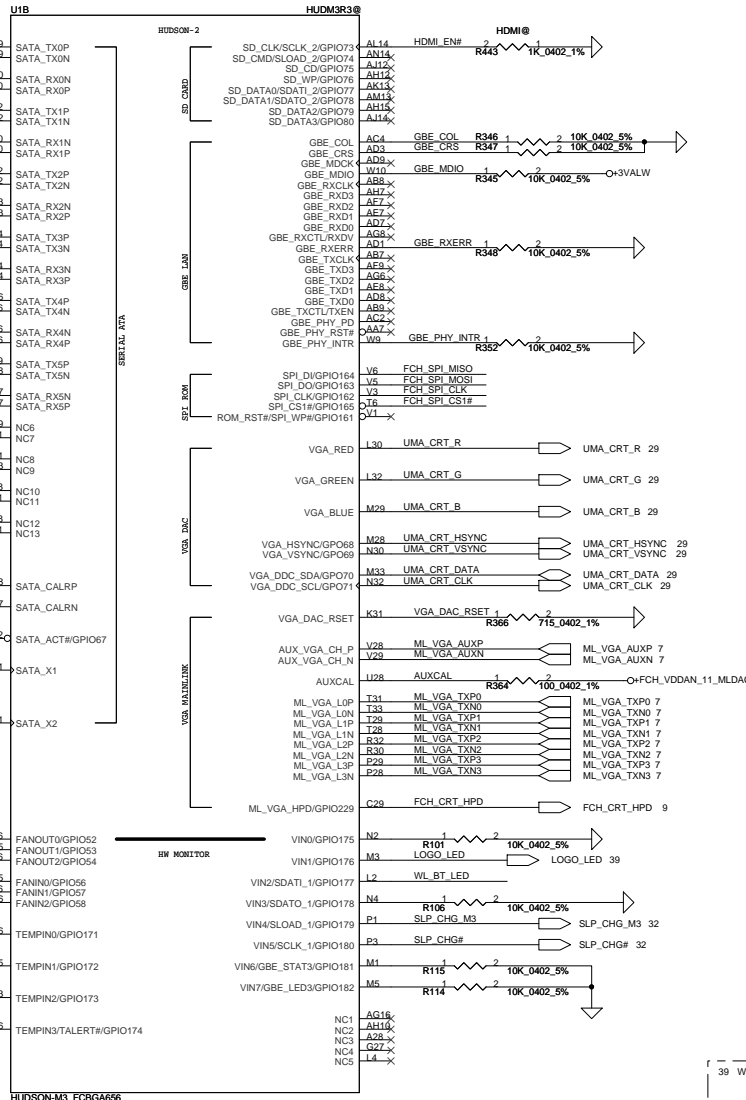
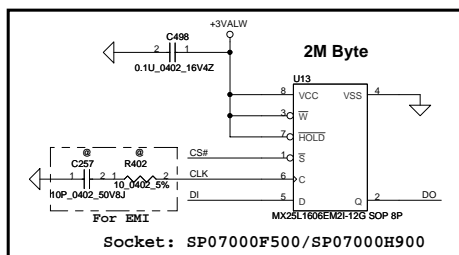
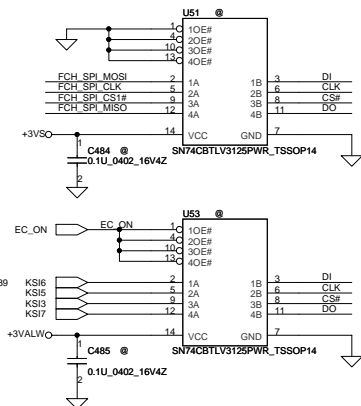
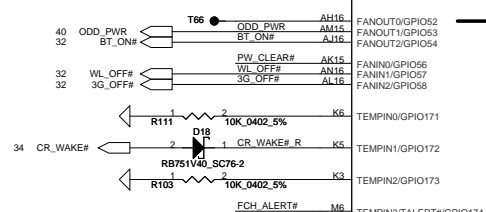
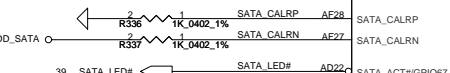
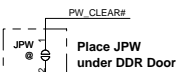
CROSS_EN# (Internal 8.2K PU)

CROSS_EN#	H	L
SKU	Non-CrossFire	CrossFire

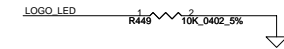
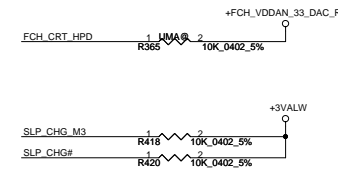
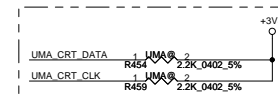
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UML link quicker.

S5_CORE_EN is for S5+ mode used to turn off +1.1VALW and +3VALW of FCH on S5+ mode



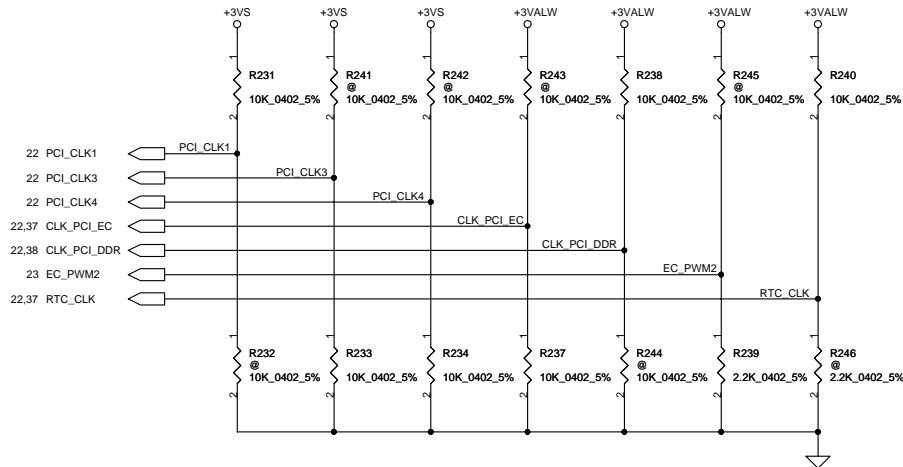


HDMI_EN# (Internal 8.2K PU)		
HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU



STRAP PINS

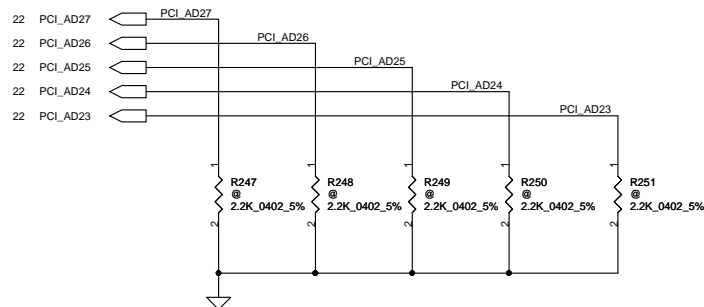
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



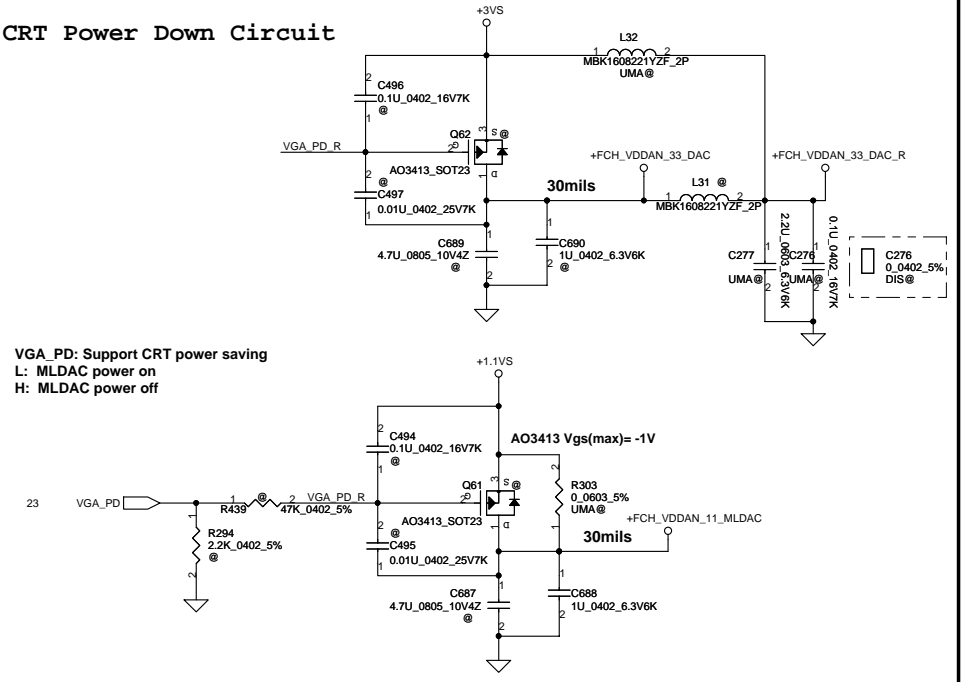
DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



CRT Power Down Circuit



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For UMA & PowerXpress

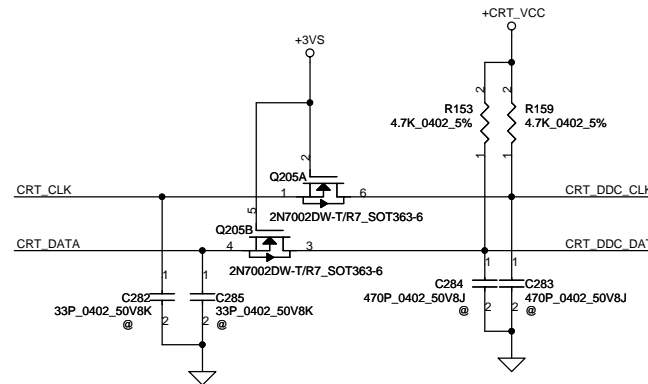
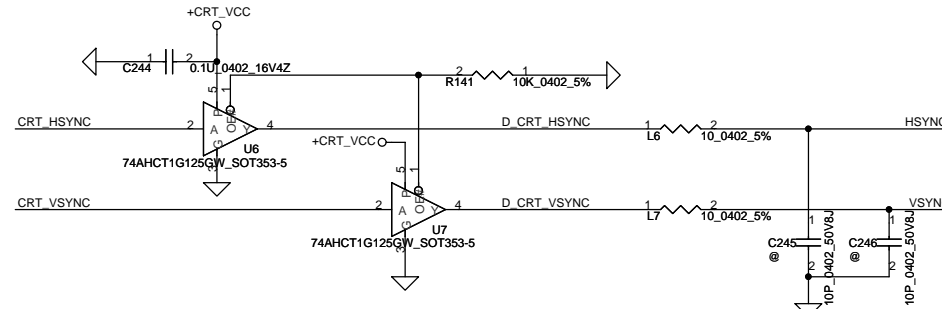
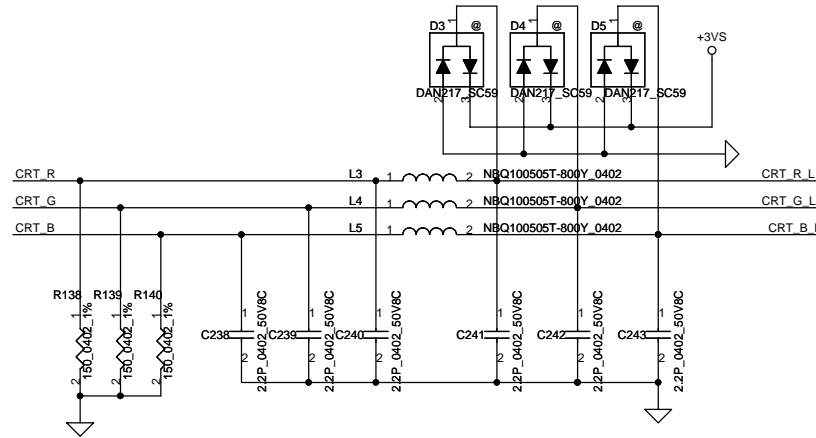
24	UMA_CRT_R	1	UMA@	2	CRT_R
		R200	0.0402_5%		
24	UMA_CRT_G	1	UMA@	2	CRT_G
		R204	0.0402_5%		
24	UMA_CRT_B	1	UMA@	2	CRT_B
		R211	0.0402_5%		
24	UMA_CRT_HSYNC	1	UMA@	2	CRT_HSYNC
		R213	0.0402_5%		
24	UMA_CRT_VSYNC	1	UMA@	2	CRT_VSYNC
		R235	0.0402_5%		
24	UMA_CRT_CLK	1	UMA@	2	CRT_CLK
		R236	0.0402_5%		
24	UMA_CRT_DATA	1	UMA@	2	CRT_DATA
		R261	0.0402_5%		

Close to CRT Connector

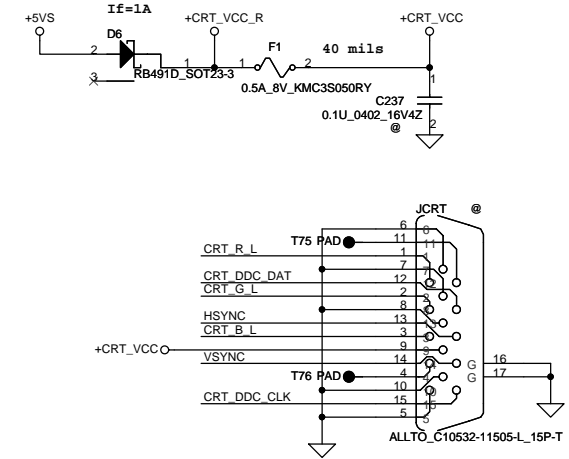
For DISCRETE

13	VGA_CRT_R	1	DIS@	2	CRT_R
		R178	0.0402_5%		
13	VGA_CRT_G	1	DIS@	2	CRT_G
		R181	0.0402_5%		
13	VGA_CRT_B	1	DIS@	2	CRT_B
		R167	0.0402_5%		
13	VGA_CRT_HSYNC	1	DIS@	2	CRT_HSYNC
		R177	0.0402_5%		
13	VGA_CRT_VSYNC	1	DIS@	2	CRT_VSYNC
		R179	0.0402_5%		
13	VGA_CRT_CLK	1	DIS@	2	CRT_CLK
		R209	0.0402_5%		
13	VGA_CRT_DATA	1	DIS@	2	CRT_DATA
		R256	0.0402_5%		

Close to CRT Connector

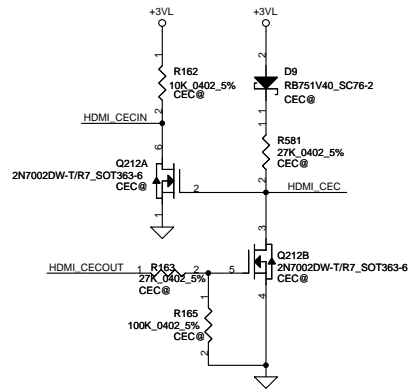


CRT CONNECTOR

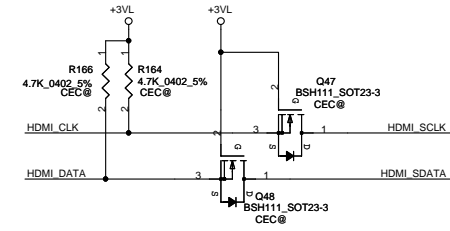
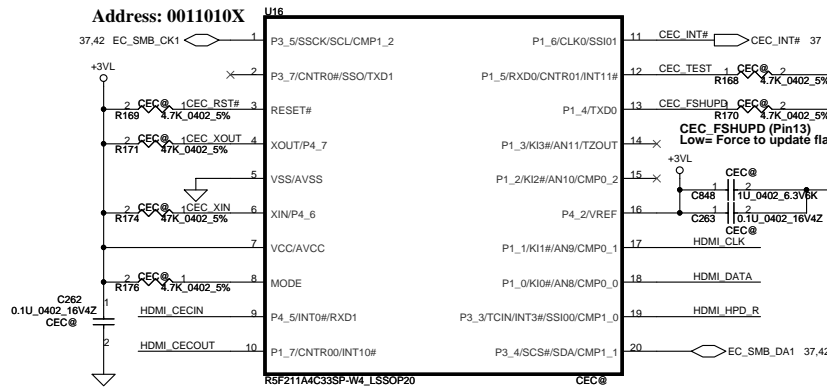


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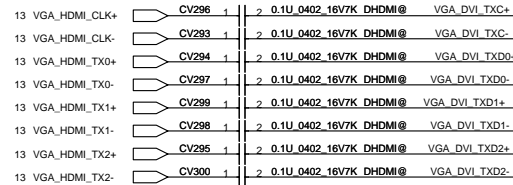
HDMI CEC Controller



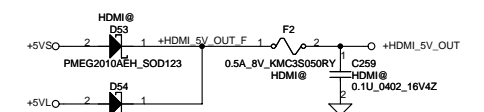
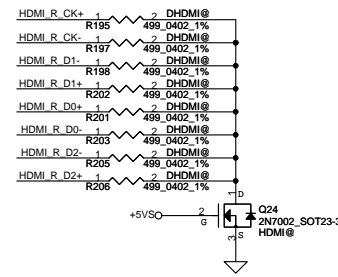
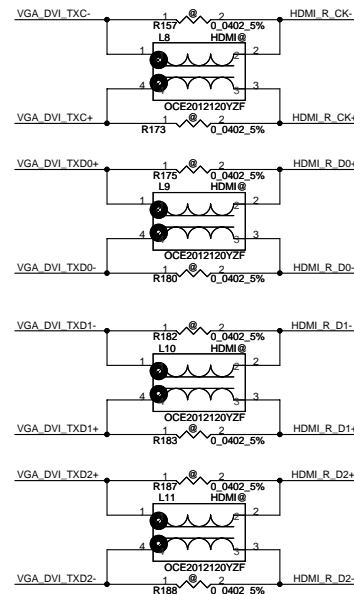
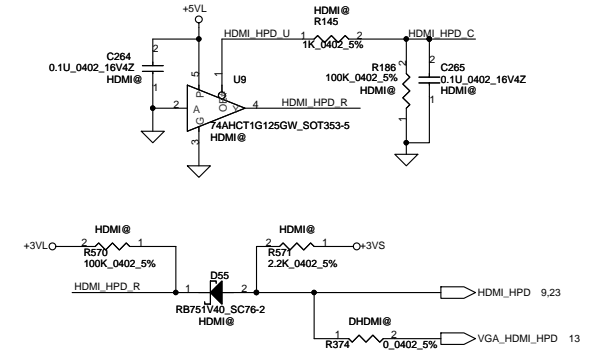
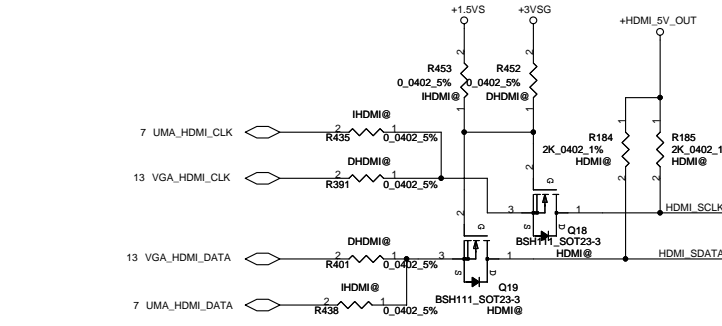
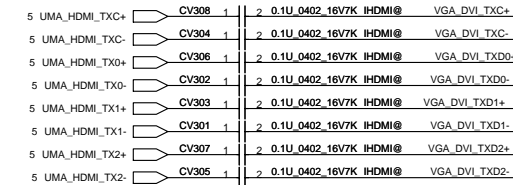
Address: 0011010X



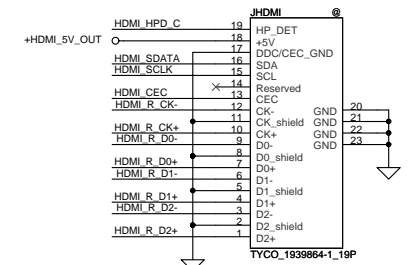
For DISCRETE



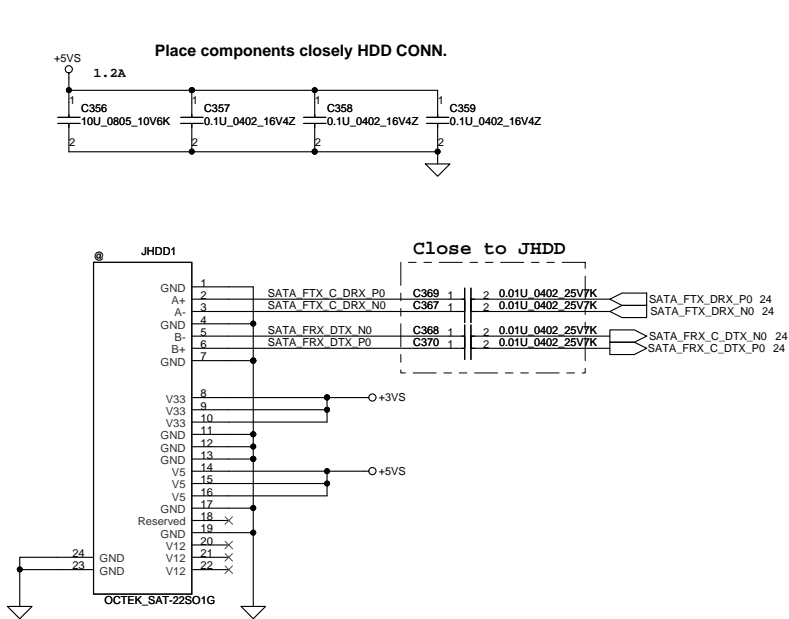
For UMA & PowerXpress



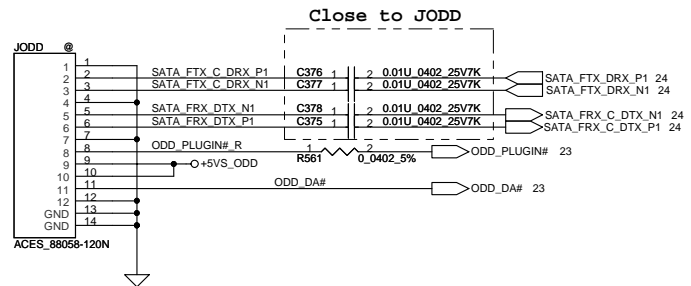
HDMI Connector



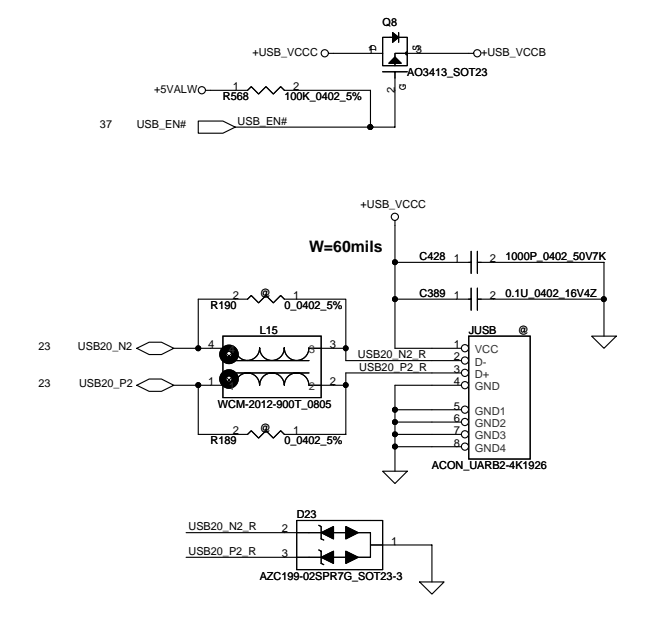
SATA HDD Conn.



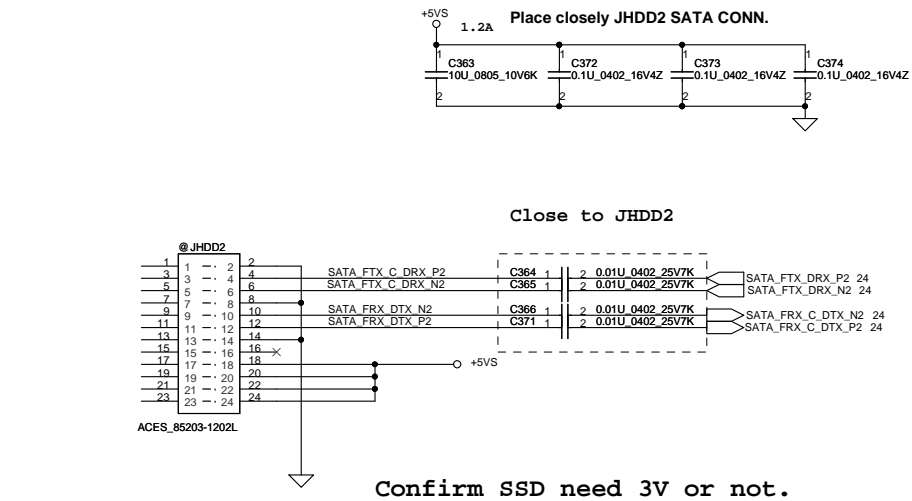
SATA ODD Conn.



USB Board@ Left Side

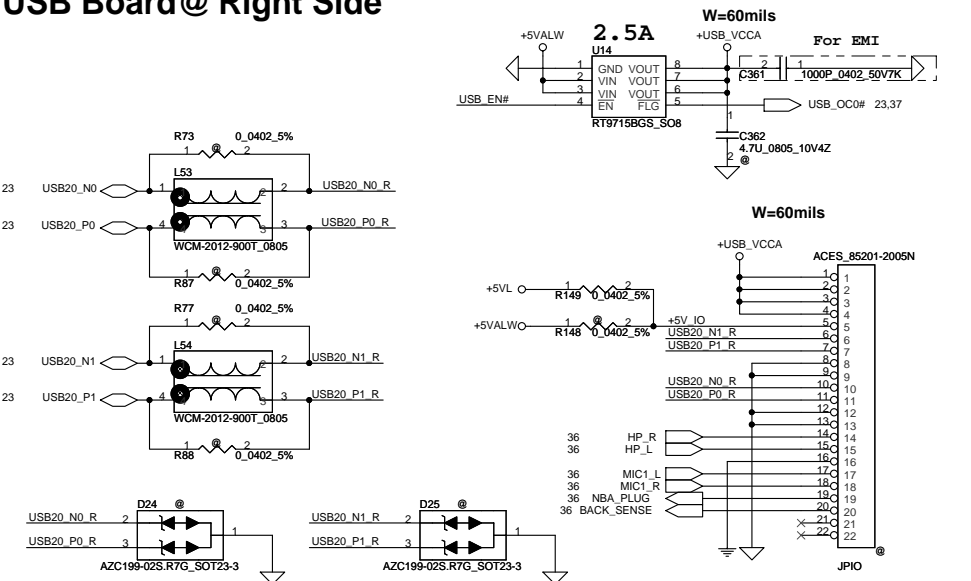


SATA 2nd HDD Conn.



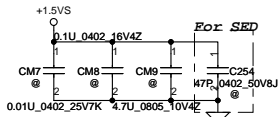
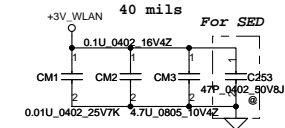
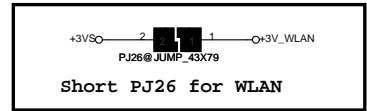
Confirm SSD need 3V or not.

USB Board@ Right Side



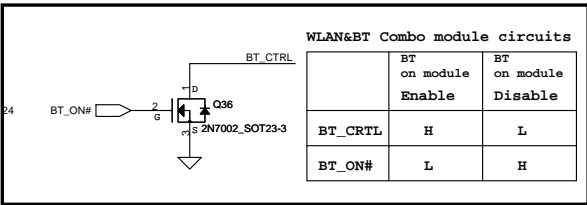
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Slot 1 Half PCIe Mini Card-WLAN



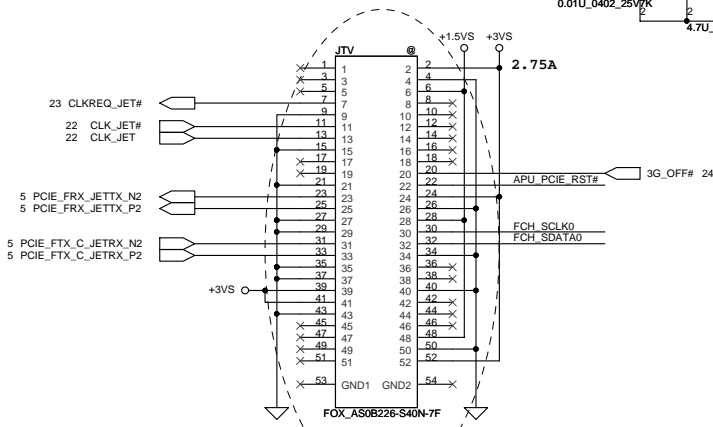
WLAN&BT Combo module circuits

	BT on module	BT on module
	Enable	Disable
BT_CTRL	H	L
BT_ON#	L	H

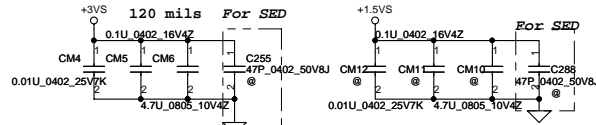


Slot 2 Half PCIe Mini Card- JET

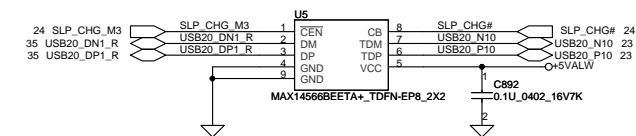
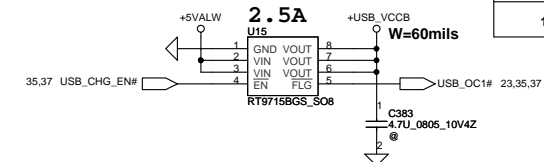
Remove 3G/TV tuner



Need to double check JET pin define



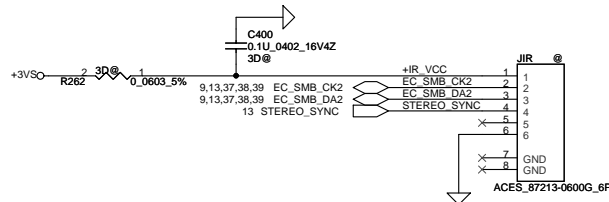
USB Sleep & Charge: Auto-Mode Mode3



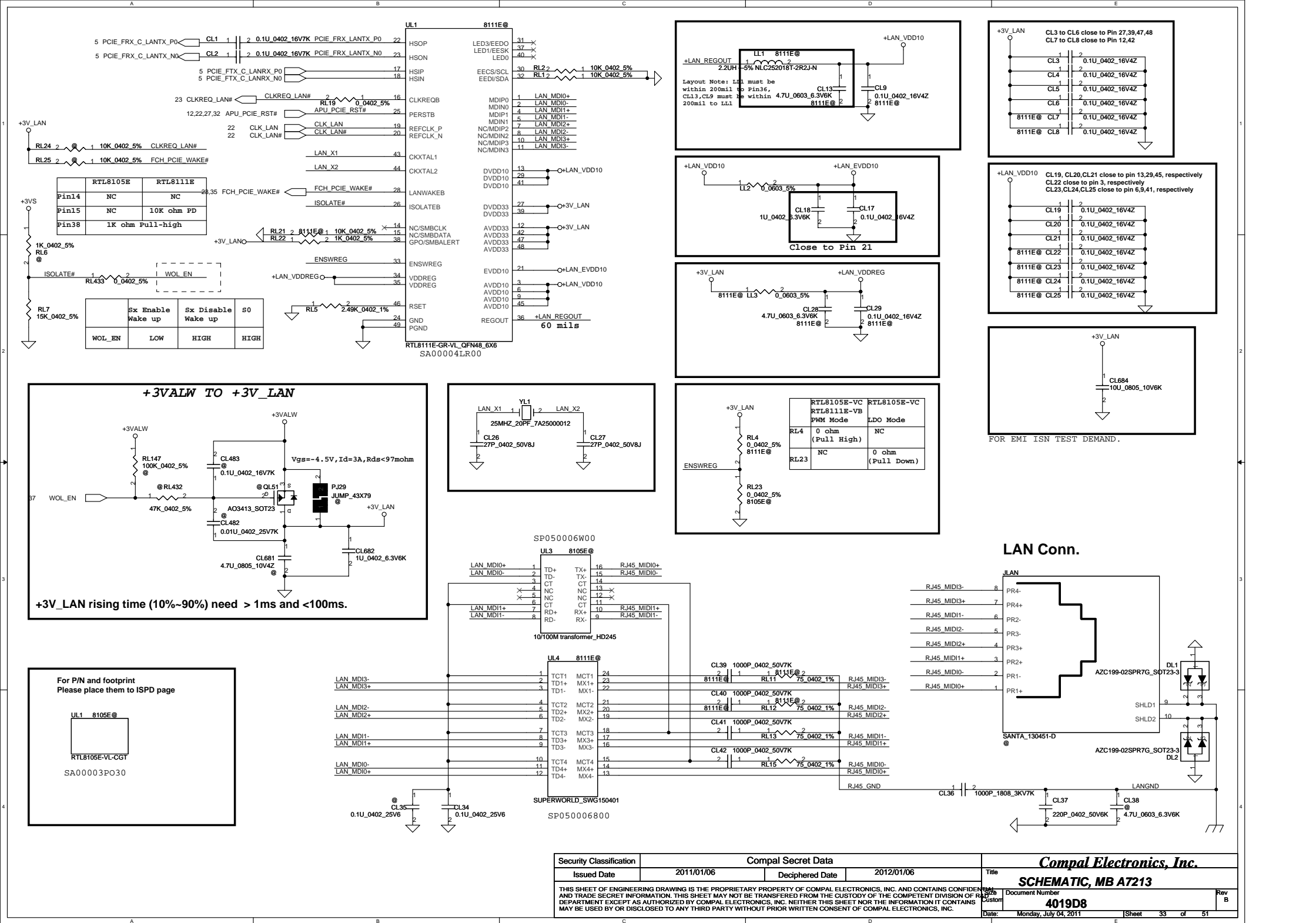
MAX14566B

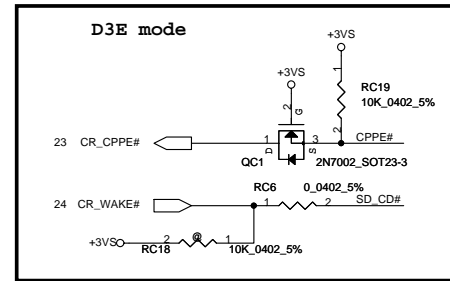
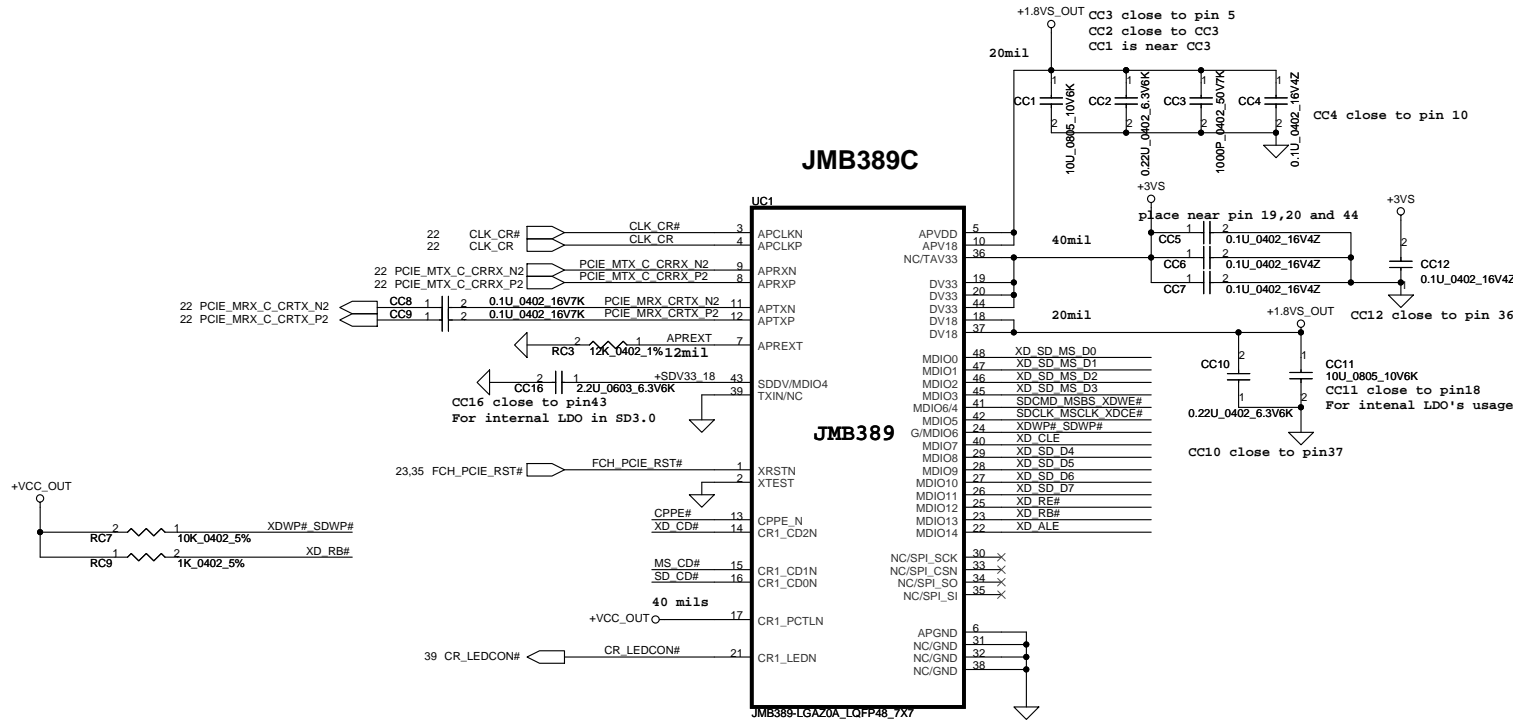
CB SLP_CHG#	CEN# SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

IR Emitter Connector

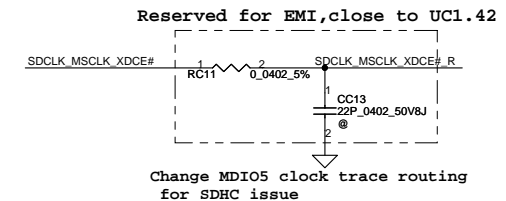
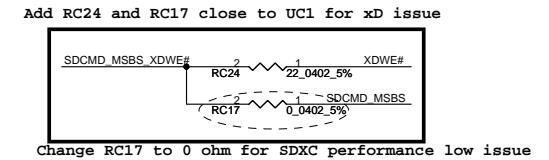
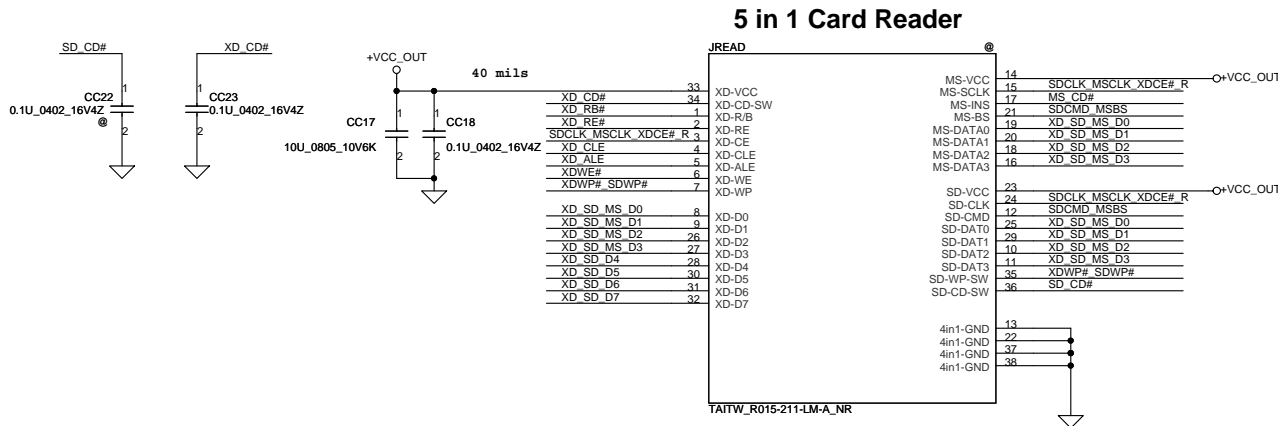


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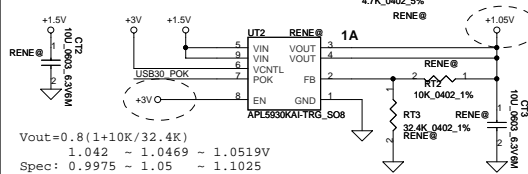




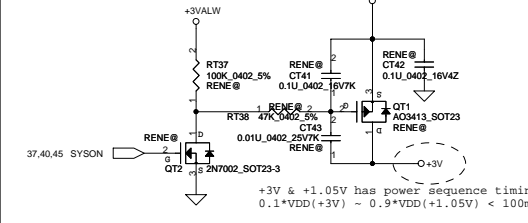
Pin name	Power On Strapping setting	
	High	Low
MDIO7	on-board	add-in card
MDIO14	CR_LEDCON# high active	CR_LEDCON# low active



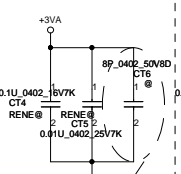
+1.5V to +1.05V Transfer



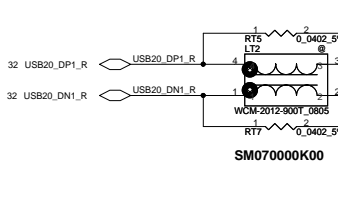
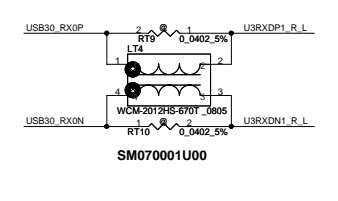
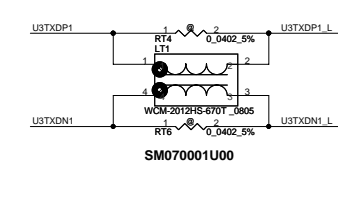
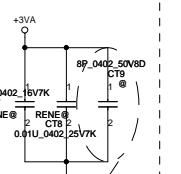
+3VALW to +3V Transfer



Close to U102.D7

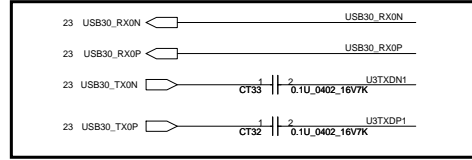


Close to U102.P13

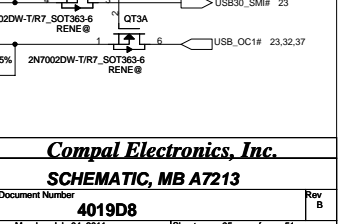
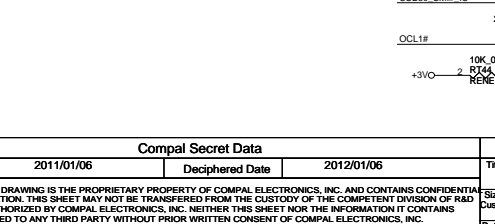
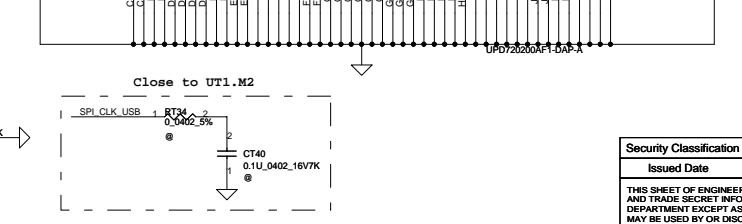
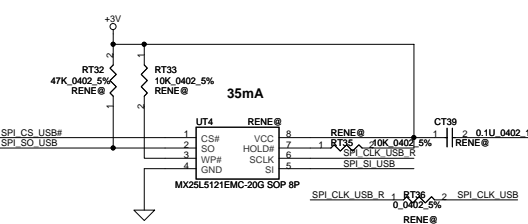
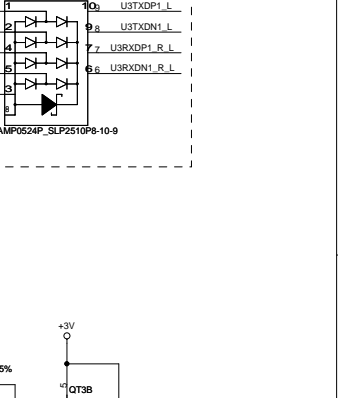
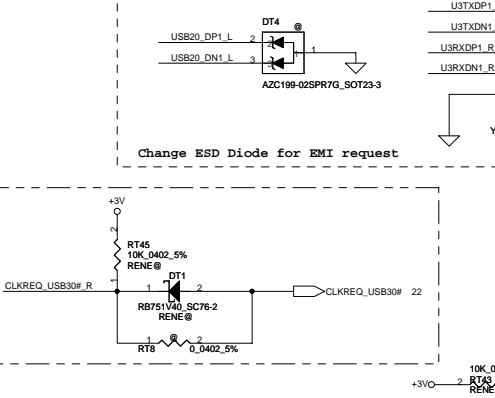
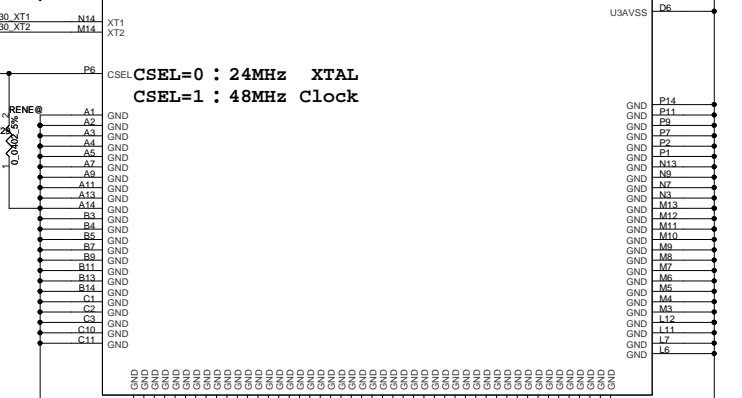
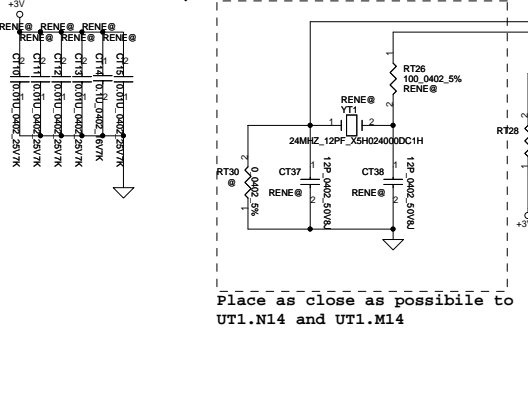
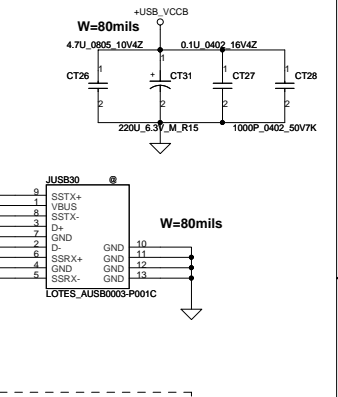
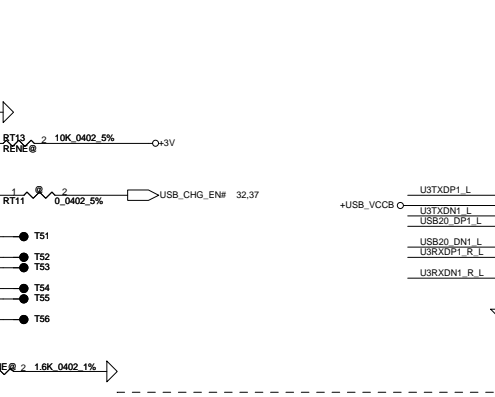
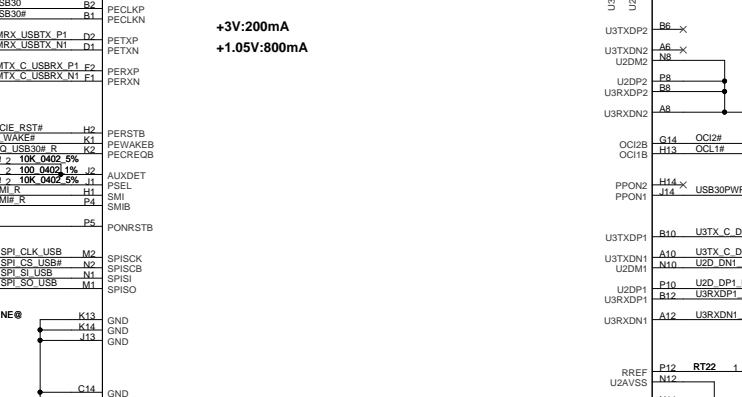
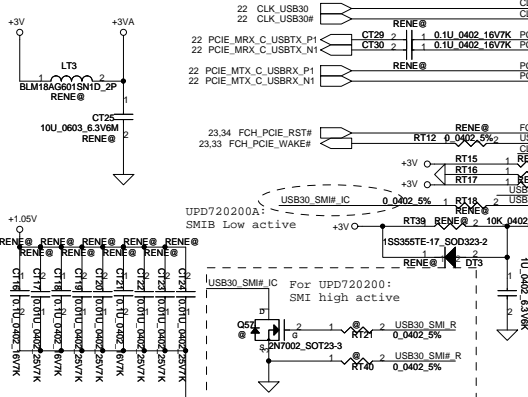


Co-Layout with Hudson M3 internal USB3.0

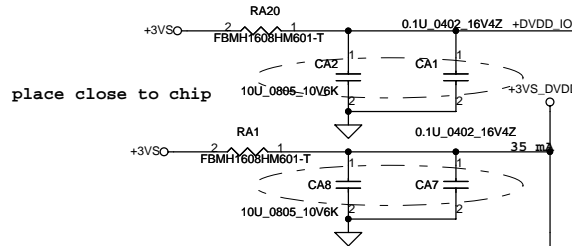
Place co-layout resistors close to UT1



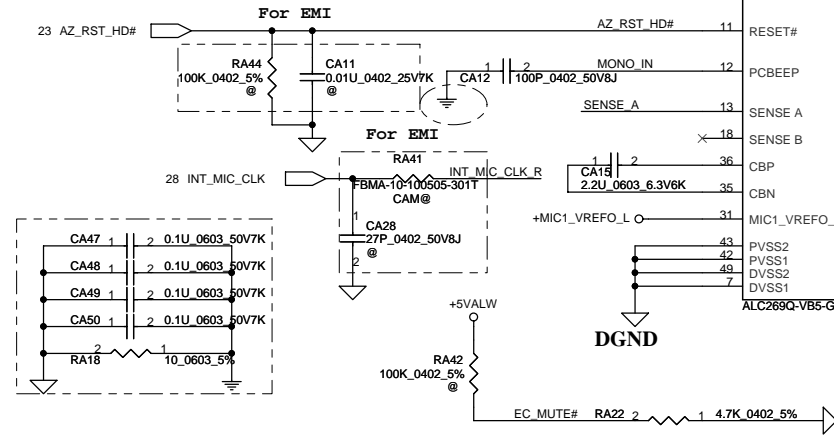
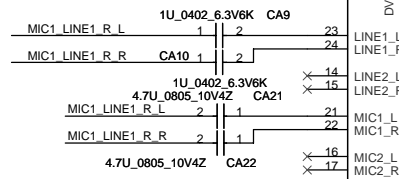
W=80mils



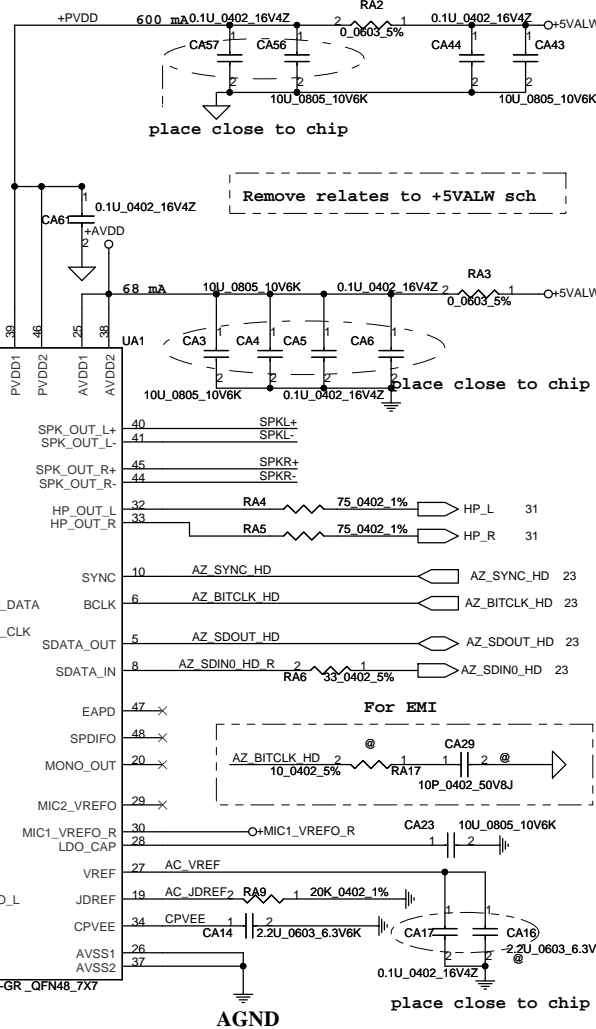
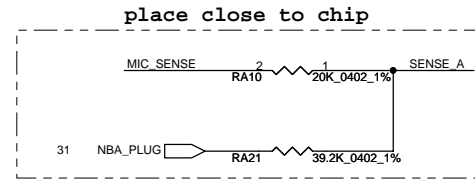
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2011/01/06		2012/01/06		Compal Electronics, Inc.	
2012/01/06		2012/01/06		SCHEMATIC, MB A7213	
2012/01/06		2012/01/06		4019D8	
2012/01/06		2012/01/06		Monday, July 04, 2011	
2012/01/06		2012/01/06		Sheet 35 of 51	



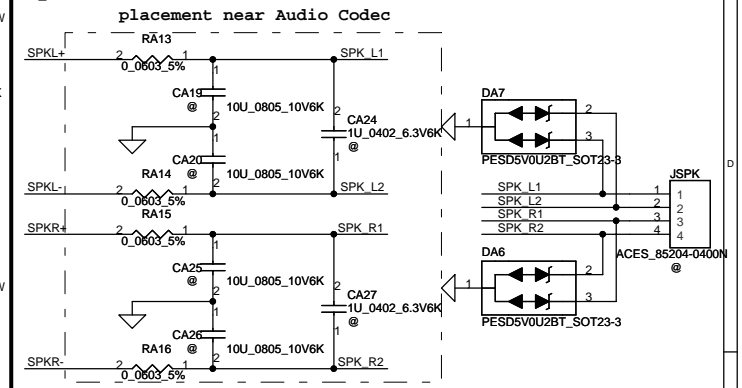
Ext. Mic/LINE IN



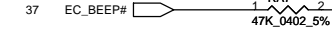
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



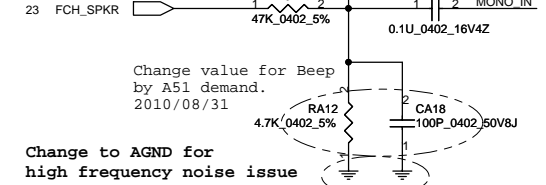
Speaker Connector



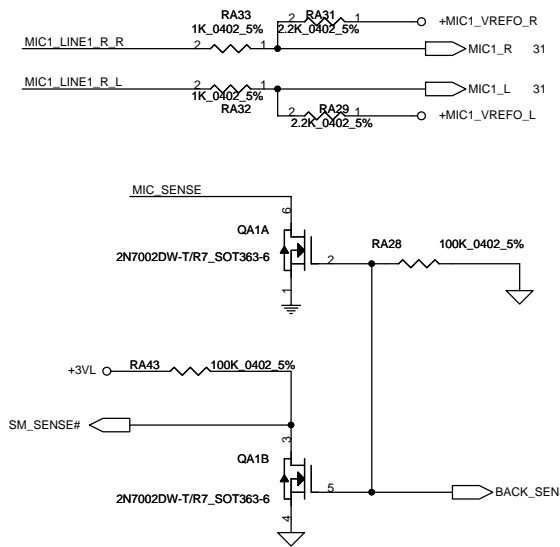
EC Beep



PCI Beep

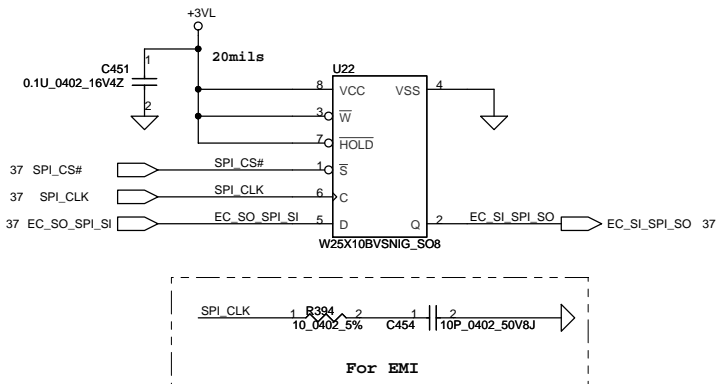


Ext.MIC/LINE IN JACK



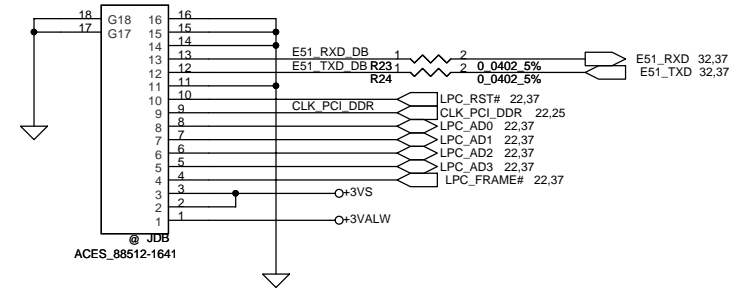
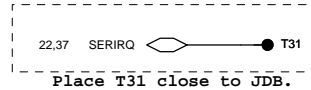
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SPI Flash (128KB)



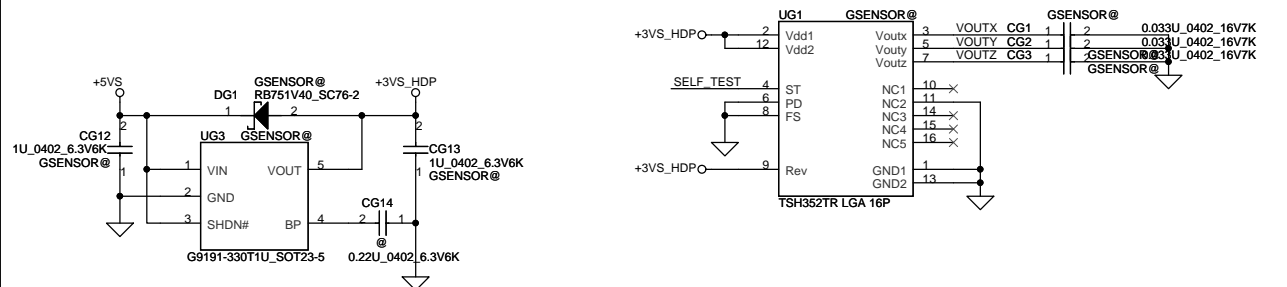
LPC Debug Port

Place JDB under DDR DIMM.

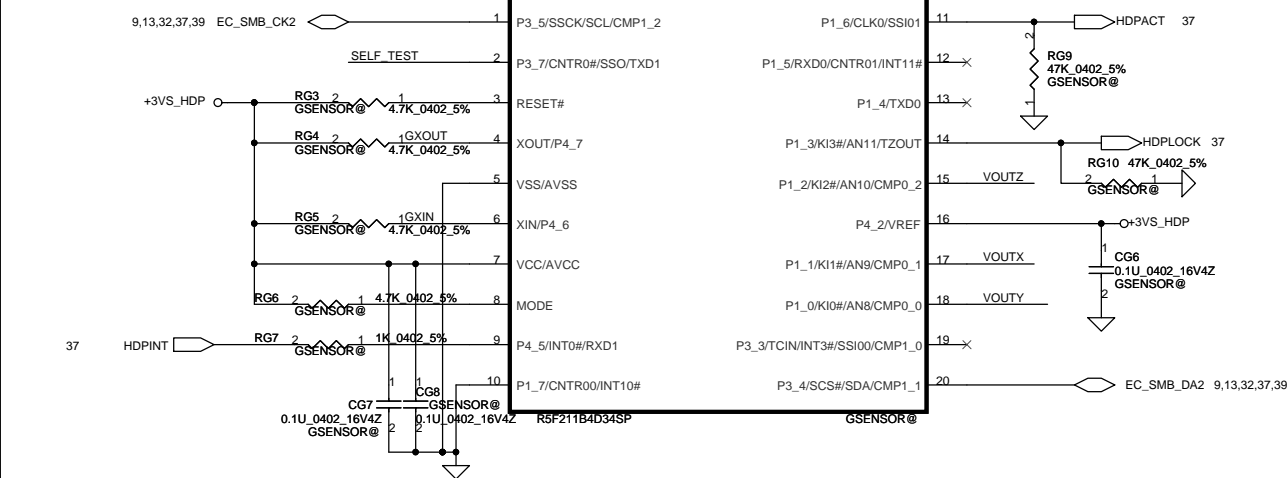


G-Sensor

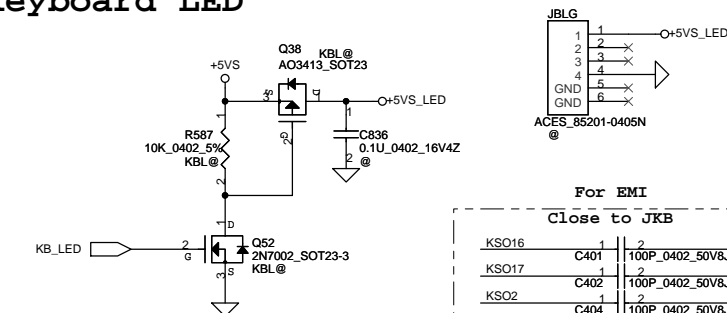
Place UG1 on TOP Layer



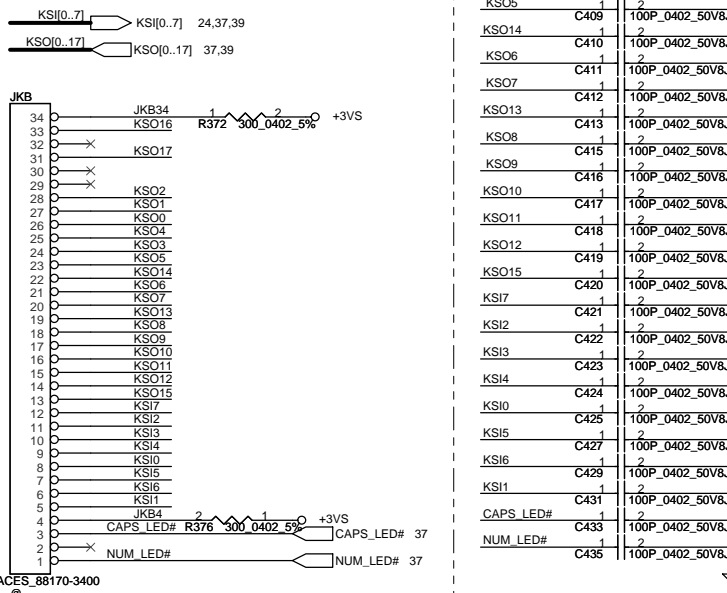
Place UG1 on TOP Layer



Keyboard LED

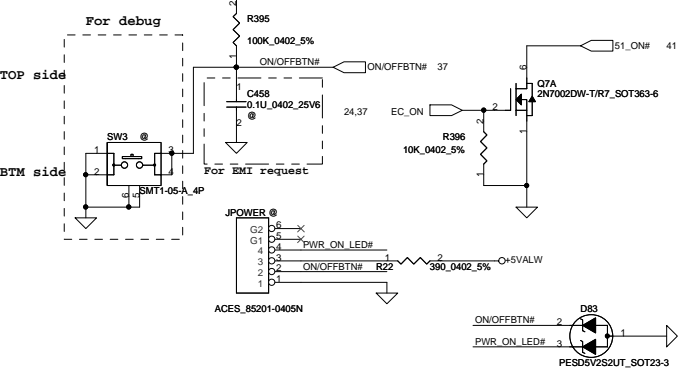


KEYBOARD CONN.

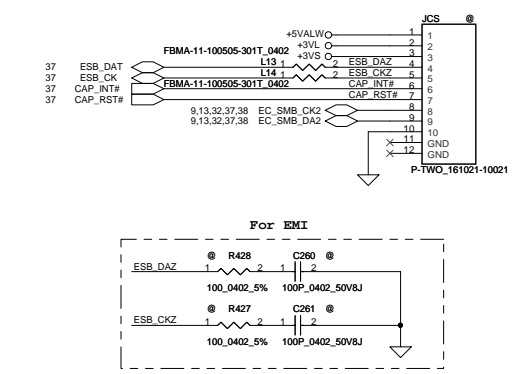


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				Document Number				B			
				4019D8							
Date:				Monday, July 04, 2011				Sheet			
				38				of			
				51							

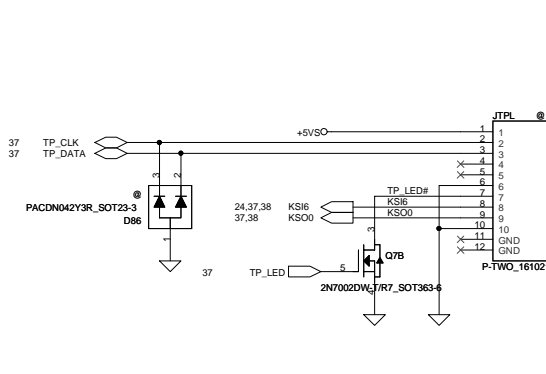
Power Button



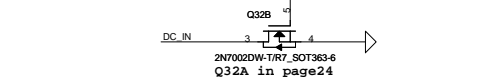
Caps Sensor/Light Sensor Conn.



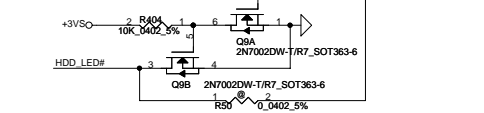
Touchpad & Light Pipe Connector



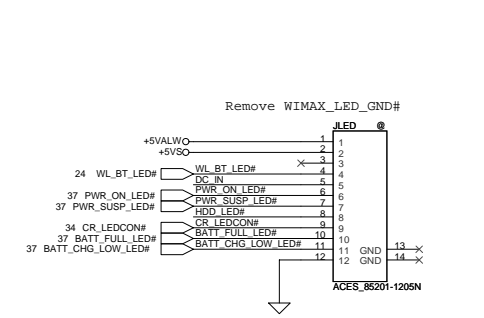
DC-IN LED



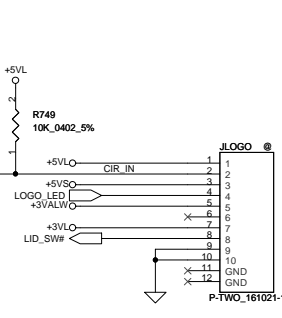
HDD LED



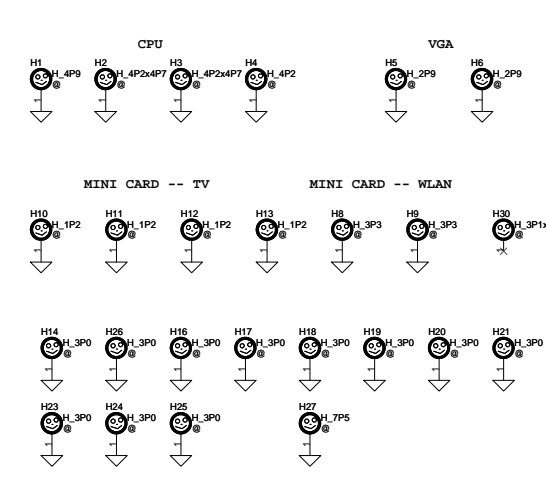
LED/B Connector



LOGO/B Connector



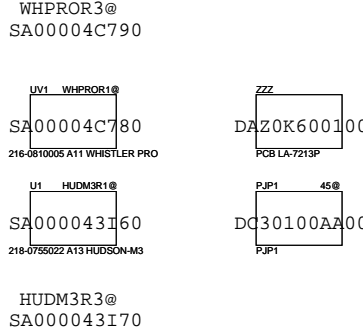
Screw Hole



PCB Federal Mark PAD

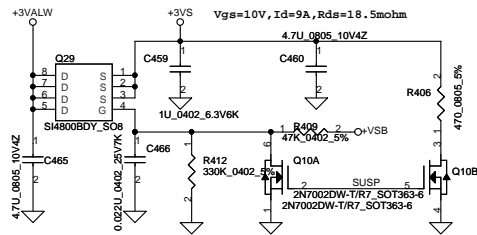


ISPD

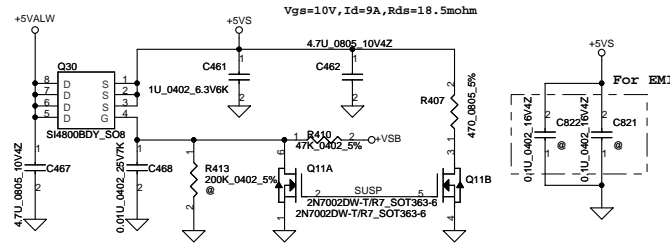


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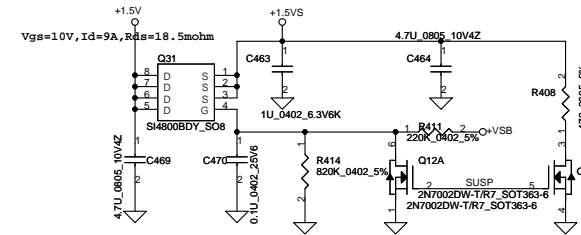
+3VALW TO +3VS



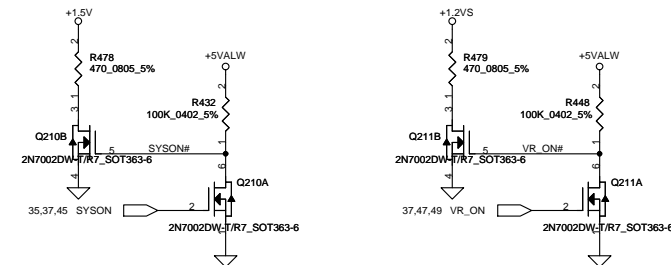
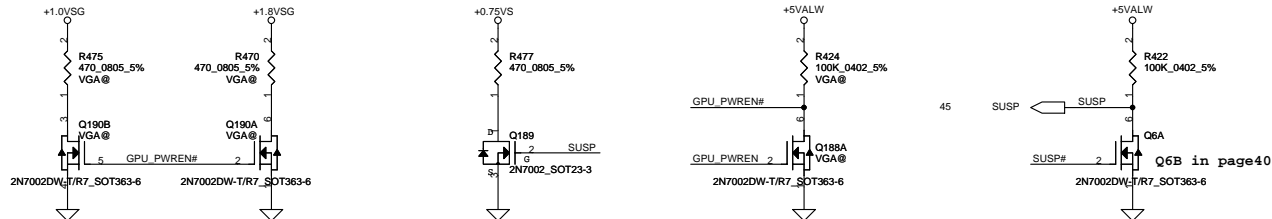
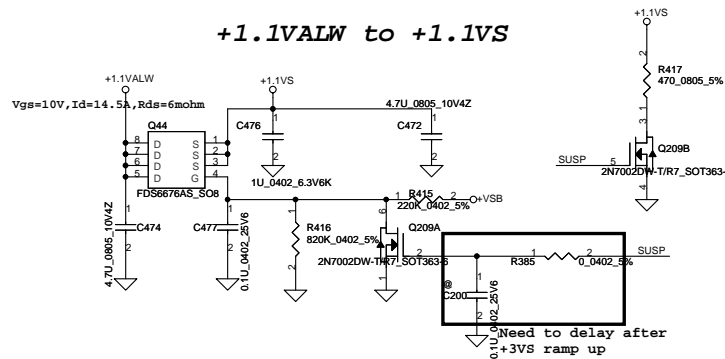
+5VALW TO +5VS



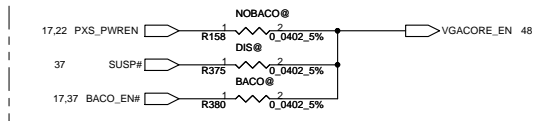
+1.5V to +1.5VS



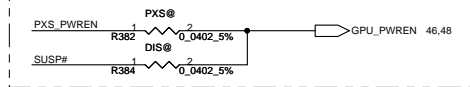
+1.1VALW to +1.1VS



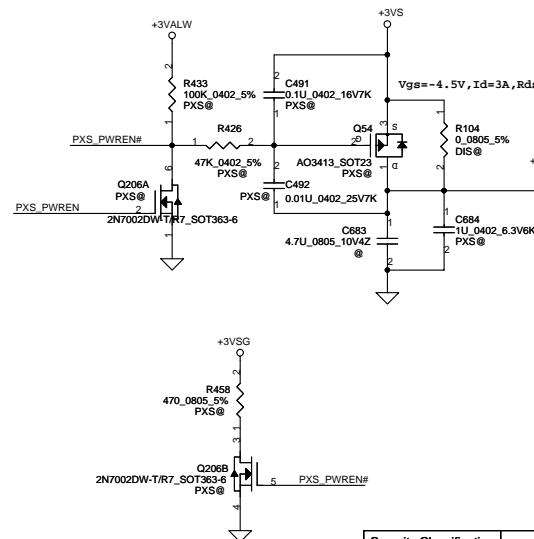
For +VGA_CORE power enable



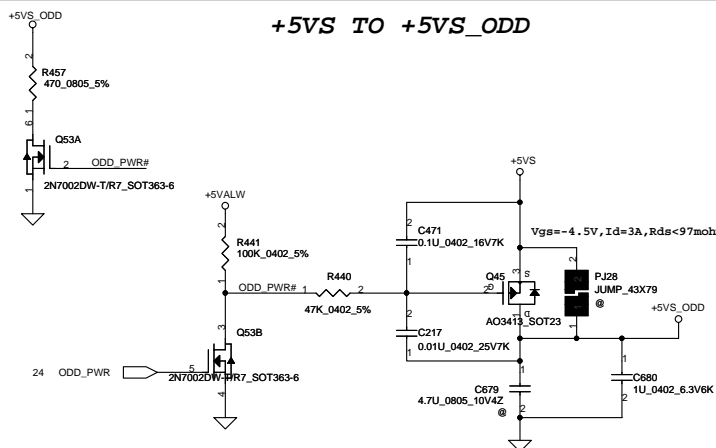
For GPU power enable



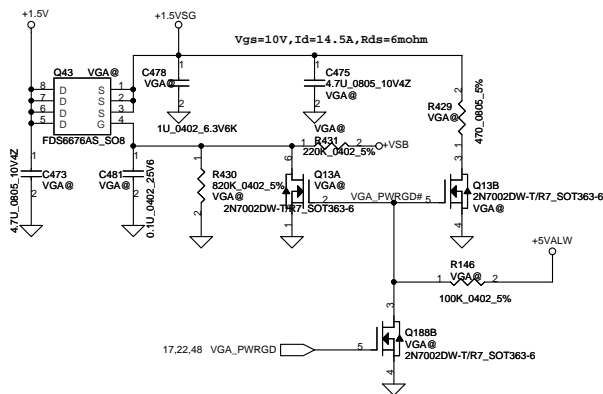
+3VS to +3VSG



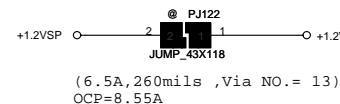
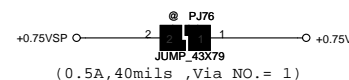
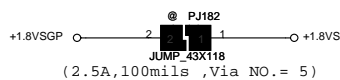
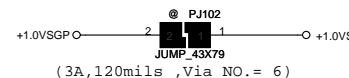
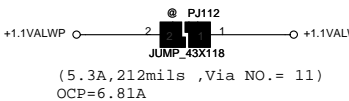
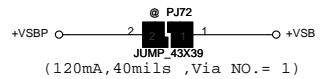
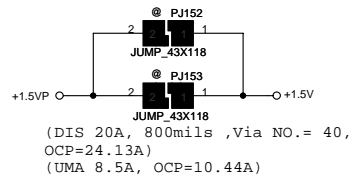
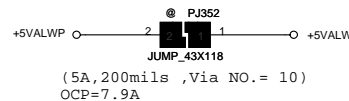
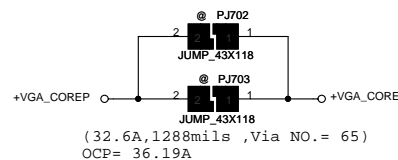
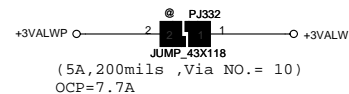
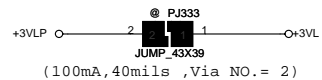
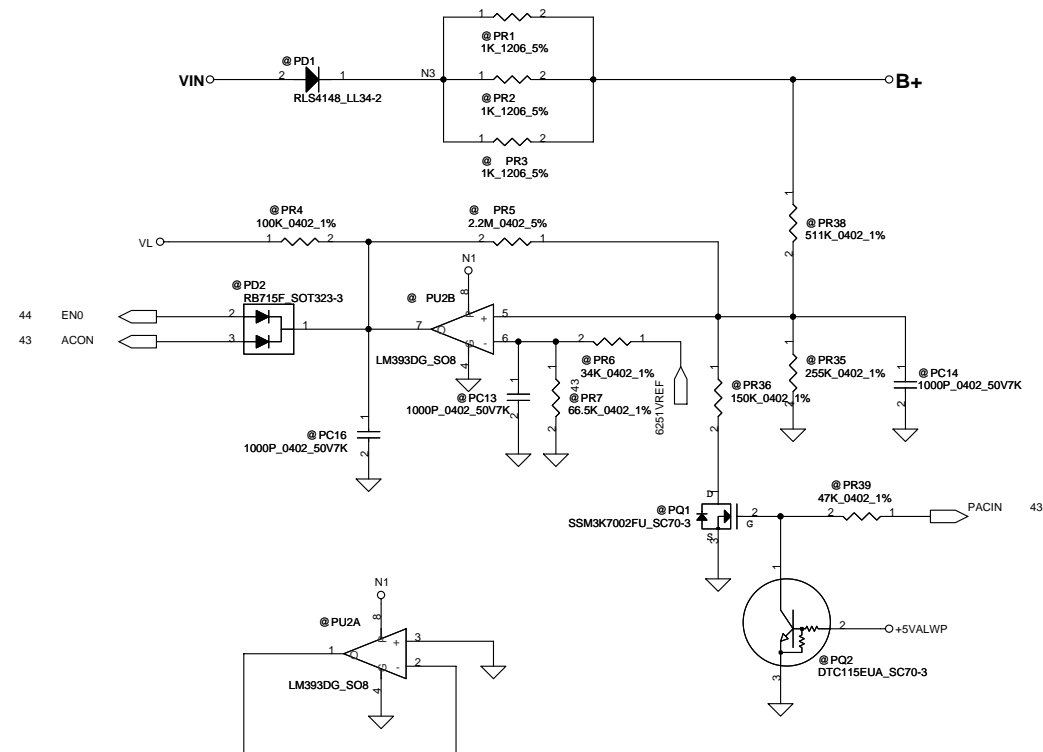
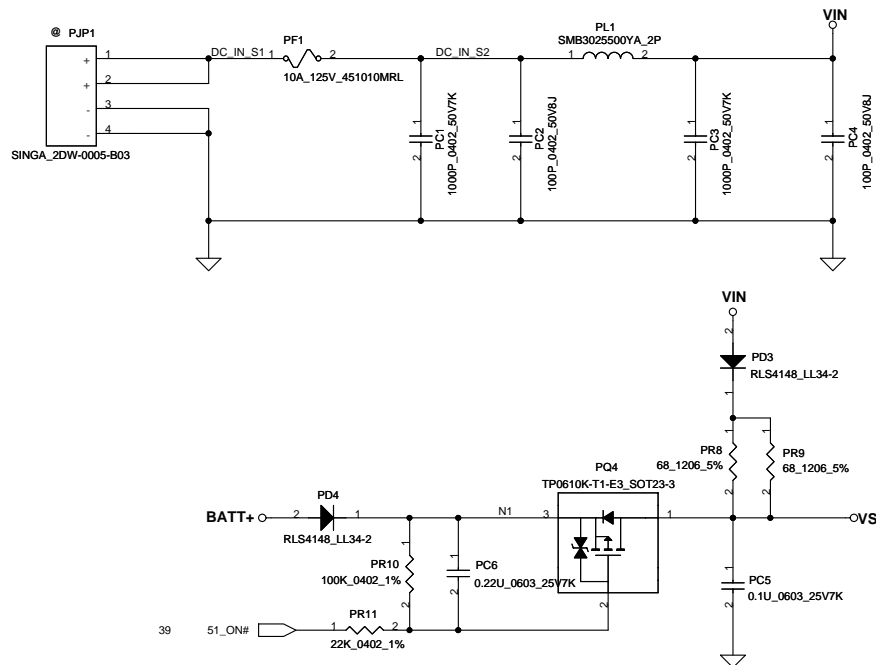
+5VS TO +5VS_ODD



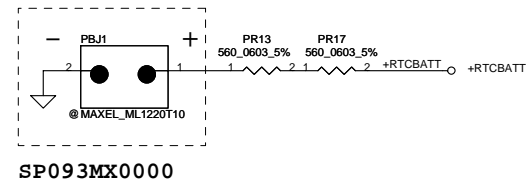
+1.5V to +1.5VSG



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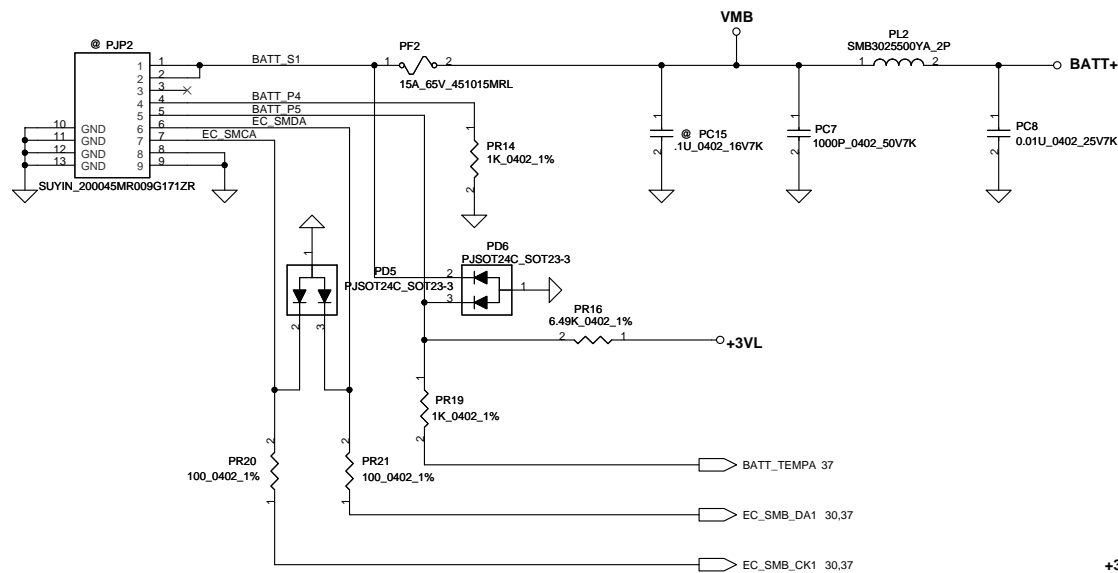
RTC Battery



ACIN

	Precharge detector		
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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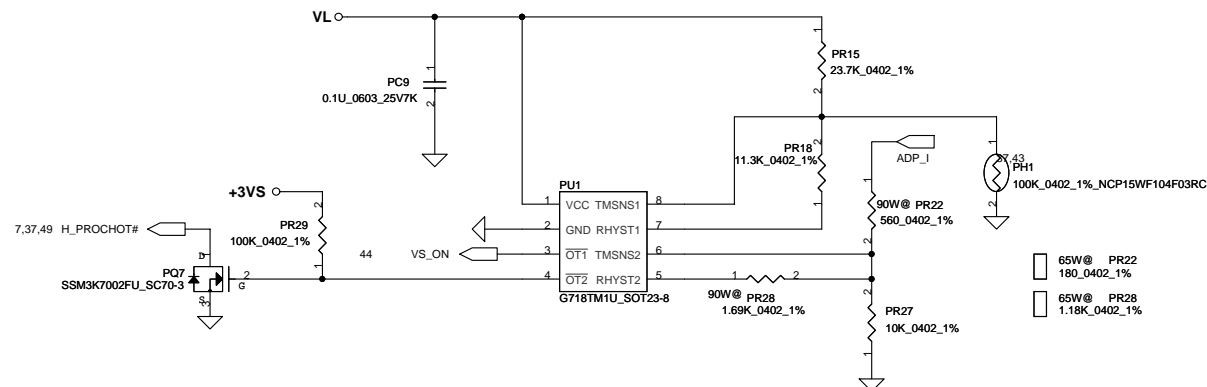


PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 56 degree C

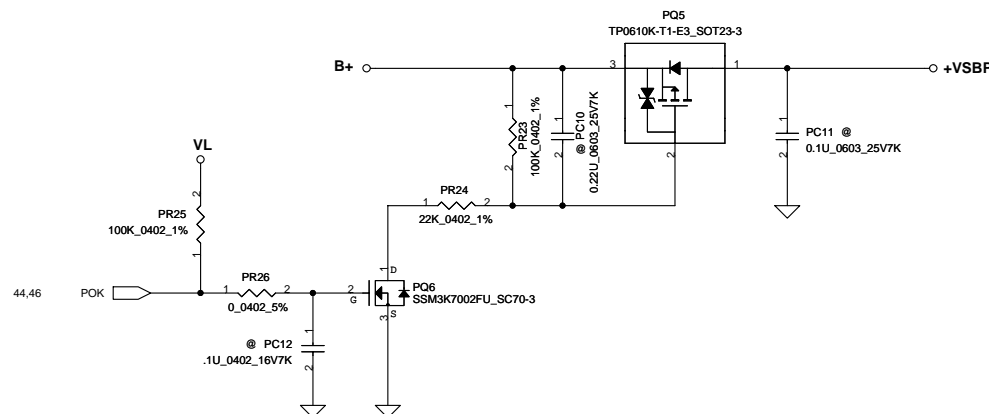
$$R_{set} = 3 * R_{tmh}$$

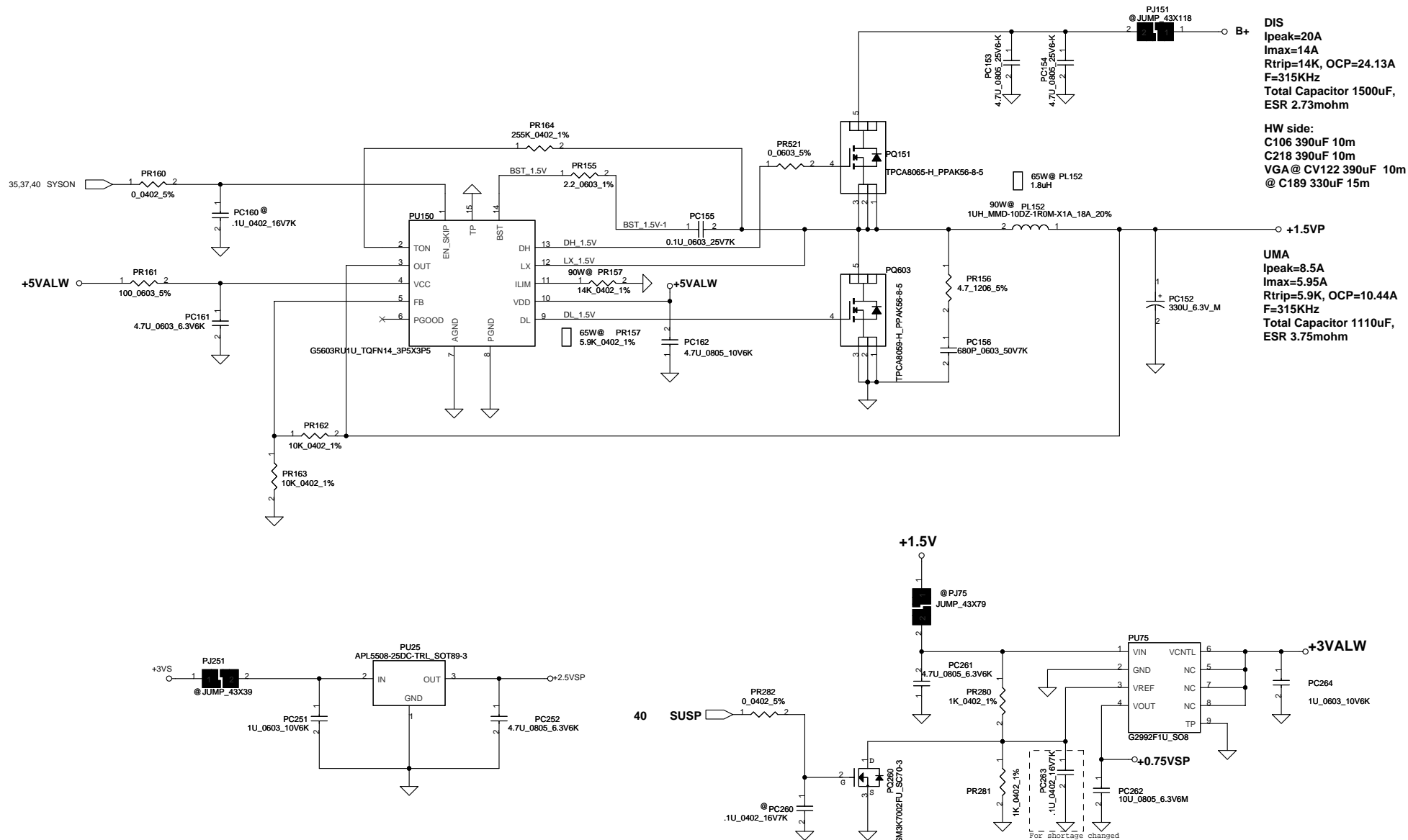
$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

Rtmh at 90C = 7.87K, Rtml at 56C = 26.1K
 $R_{set} = 3 * 7.87K = 23.61K \Rightarrow 23.7K$
 $R_{hyst} = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K \Rightarrow 11.3K$

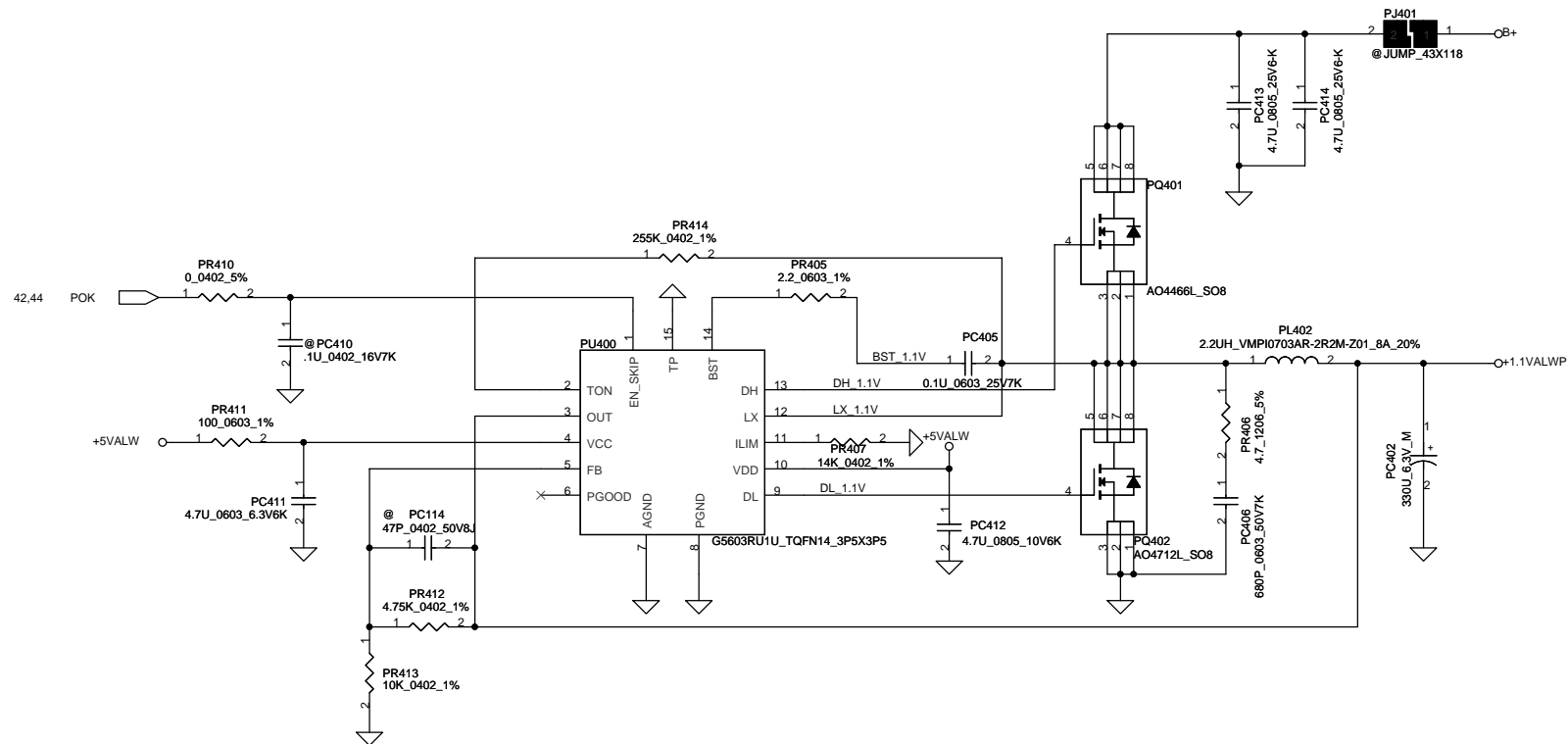


Adaptor protection				
Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
90W	113.5W	1.783V	86.4W	1.357V
65W	71.8W	1.5V	62.44W	1.3V

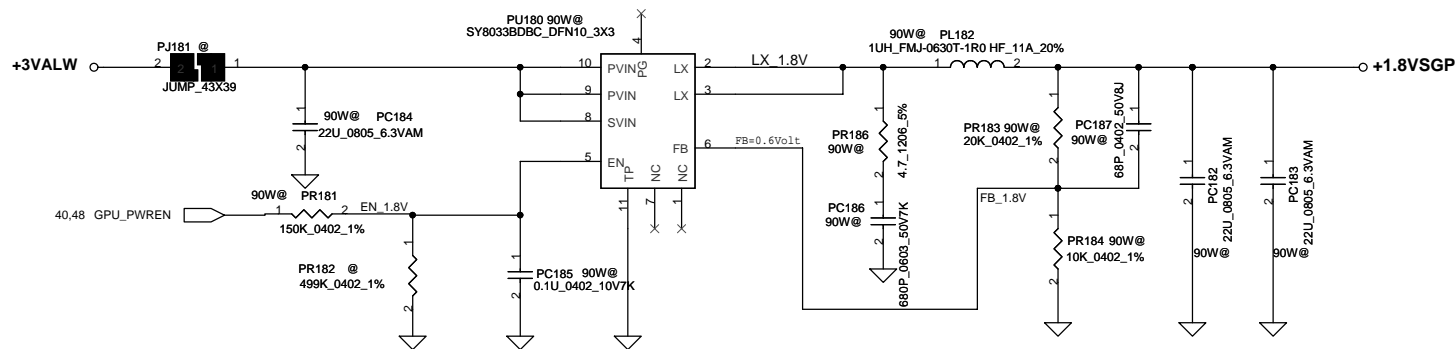




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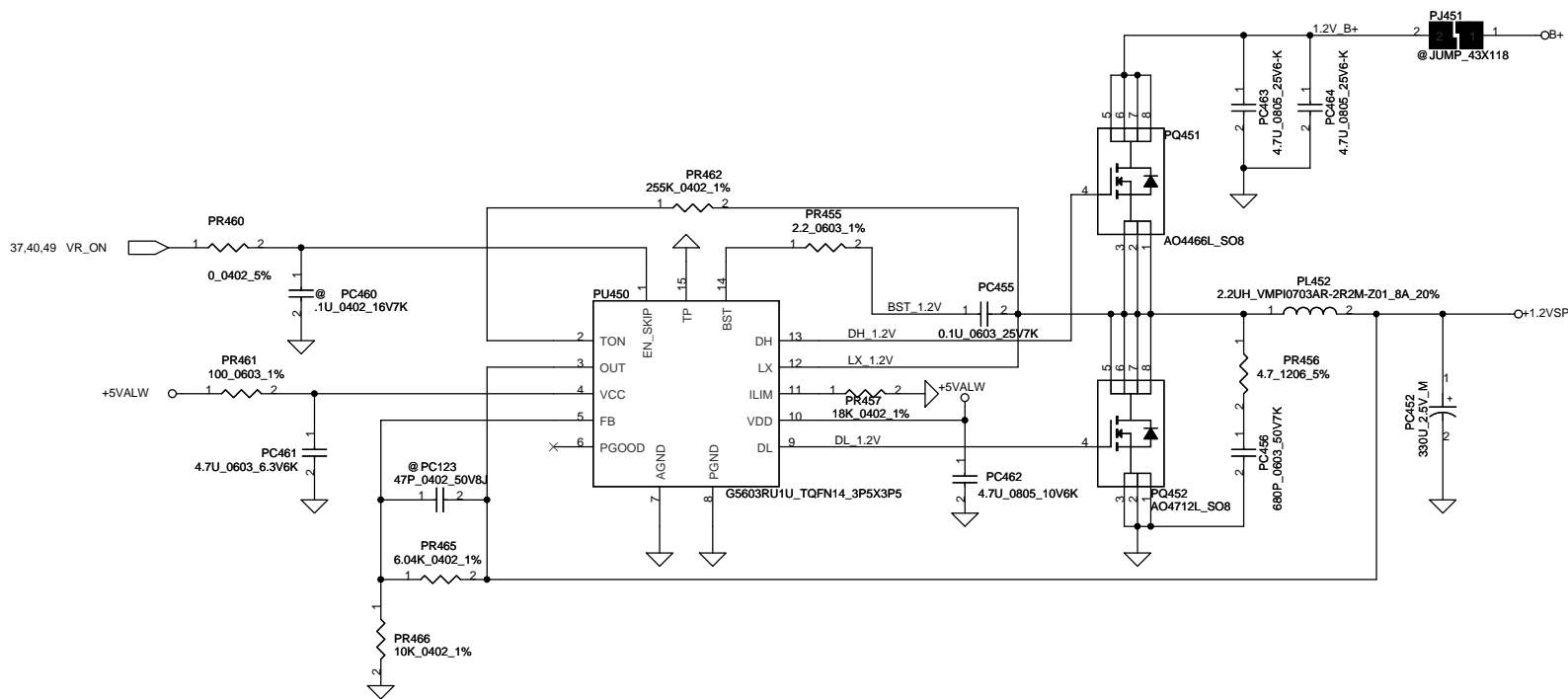


Ipeak=5.3A
I_{max}=3.71A
R_{trip}=14K, OCP=6.64A
F=315KHz
Total Capacitor 330uF,
ESR 15mohm



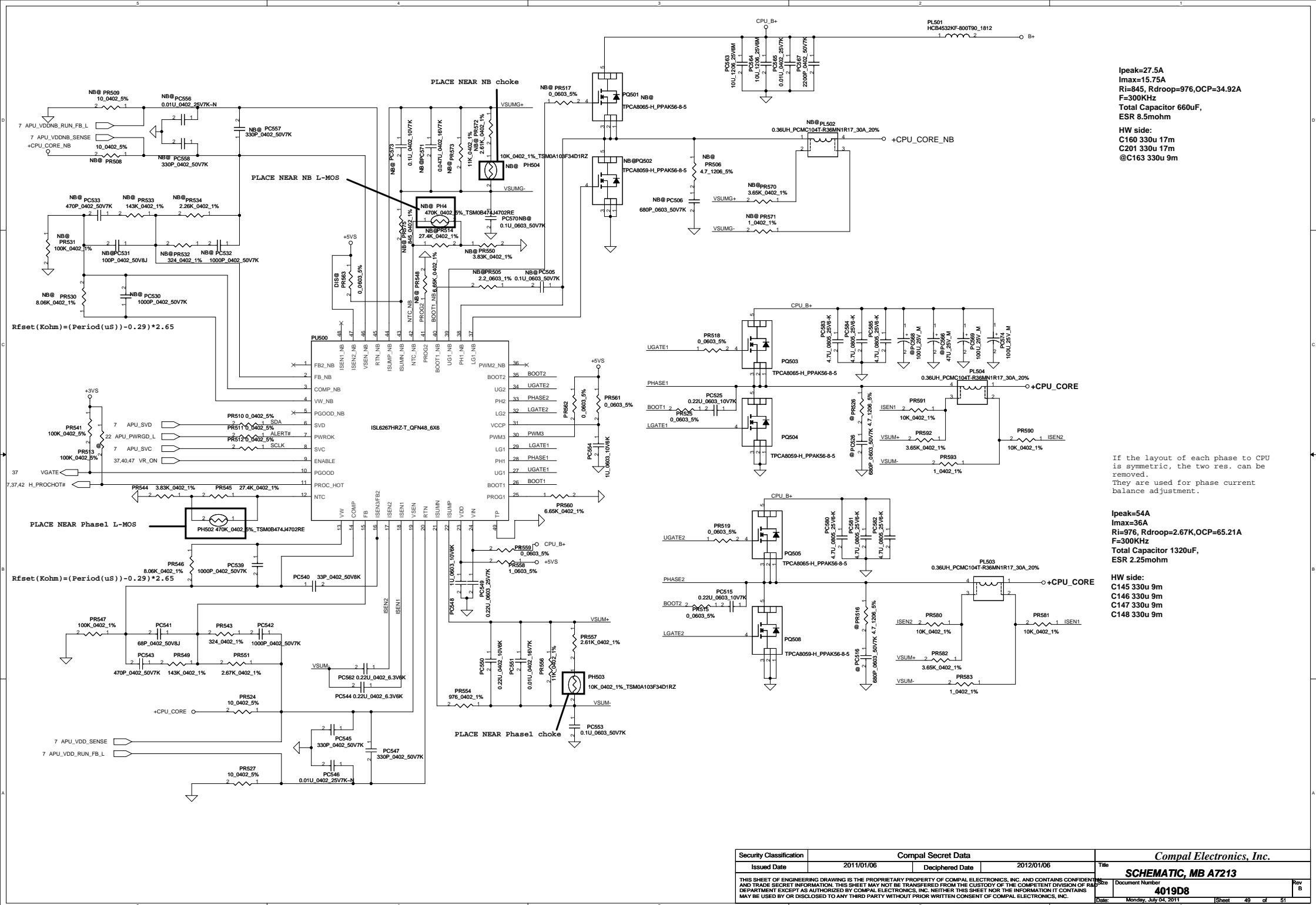
Ipeak=2.5A
ILIM = 4A
F=1MHz
Total Capacitor 44uF,

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I_{peak}=6.5A
I_{max}=4.55A
R_{trip}=18K, OCP=8.37A
F=315KHz
Total Capacitor 720uF,
ESR 6mohm
HW side:
C130 390uF 10m

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Ipeak=27.5A
 Imax=15.75A
 Ri=845, Rdroop=976, OCP=34.92A
 F=300KHz
 Total Capacitor 660uF,
 ESR 8.5mohm

HW side:
 C160 330u 17m
 C201 330u 17m
 @C163 330u 9m

If the layout of each phase to CPU is symmetric, the two res. can be removed.
 They are used for phase current balance adjustment.

Ipeak=54A
 Imax=36A
 Ri=976, Rdroop=2.67K, OCP=65.21A
 F=300KHz
 Total Capacitor 1320uF,
 ESR 2.25mohm

HW side:
 C145 330u 9m
 C146 330u 9m
 C147 330u 9m
 C148 330u 9m

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HW PIR (Product Improve Record)

Q { 樗蘊惇矜 \ 饒惇幹机區蛸濕葵 \ 驚掄哪EMATIC C { 樗惇鷗躍E LIST

REVISION C { 樗惇鷗躍E: 0.1 TO 0.2

Item	Date	Page	Solution	Request
1.	3/17	P23	Remove level-shifter for ODD_PLU { 鯨確鷗耳	ODD has internal 1K pull-down
2.	3/17	P34	Add level-shifter for CR_CPPE#	For leakage issue
3.	3/17	P23	Change { 樗縵置確焂躑PD to { 鯨矜 矜鷗鶻蛸鼻耳 \ 踰睨 \ 葵碑鯨erve { 鯨矜 矜鷗鶻蛸狒耳 \ \ \ \ \ \ \ \ \ \ 躑EVENT9# has issue	
4.	3/17	P24	Change LO { 鯨鶻焂饒矜縵 \ 蟲簾 \ 躑PI0176 and WL_BT_LED to { 鯨葵確鶻蛸机机 \ \ \ \ \ \ \ \ \ 淳簾葵 \ 饒矜縵 \ 疴黴 鯨灼 \ 曉鯨表碑 \ 疴蟲碑葵 \ 尊簾設碑葵幹簾踰	
5.	3/24	P10	Add C295,C316,C324,C325	For EMI test
6.	3/28	P39	Reserve C20,C21,C229,C231~C236,C247,C251	For ESD test)
7.	3/29	P38	Change LPC debug port to 16pins connector	To support new debug card
8.	3/30	P07	Add R70,R102,R105	Pull-down for unused { 樗葵縵 \ 尊簾葵蟲

REVISION C { 樗惇鷗躍E: 0.2 TO 1.0

Item	Date	Page	Solution	Request
1.	4/15	P31	Reserve D24, D25	
2.	4/27	P22	Change R257 form 100k to 10k for leakage issue.	
3.	4/27	P37	Add BACO_EN# to EC	To inform EC { 鯨葵む \ 蟲灼碑葵聯 翟 \ 鯨碑踰鯨簾葵 \ 鯨蟲 蟲表鯨

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